Stability Analysis of PLL Influenced by Control Loops in Grid-connected Converters Under Fault Disturbance

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Abstract—When the power grid suffers from grid faults that cause phase disturbances, the grid-connected converter becomes destabilized by the interaction between the phase-locked loop (PLL) and the control loop. In this paper, the stability of the PLL affected by the control loop under transient grid faults is studied. First, the equivalent model of the PLL under the influence of the control loop is established. Then, different response processes of PLLs under the ground fault with various control parameters are qualitatively analyzed. Furthermore, a small-signal model is proposed to assess the stability of the PLL under different control loop parameters. The system poles can be calculated to show the physical origin of the instability. Finally, simulations of a three-phase 21-level modular multilevel converter (MMC) built in PSCAD and a down-scale experiment is performed to verify the parameter influence of the control loop on the PLL.

Index Terms—Control loop, grid-connected MMC, ground fault, phase-locked loop, transient stability.

I. INTRODUCTION

W ITH the increasing application of power electronic devices in the power system, operational characteristics of power systems have changed tremendously due to the introduction of such devices [1]–[4]. For example, when a fault occurs in the power grid, the fault may have an adverse influence on the operation of grid-connected converters, and then the dynamic behaviors of converters may further exacerbate the operation of the whole power system. To ensure the safe operation of power systems have received increasing attention during recent years [5]–[8].

Considering that grid faults always bring severe problems to power electronic-based power systems, such as overcurrent, overvoltage and some oscillation behaviors [9]–[11], studying how grid faults impact converters that are connected to weak AC grids becomes a popular research area [12]–[14]. From most of this research, the behaviors of phase-locked loops (PLLs) have been revealed to analyze the impact on the stability of converters [15], [16], since the PLL is adopted to detect the voltage phase at the point of common coupling (PCC) to synchronize converters to the power grid [17].

A great amount of research has been done investigating the small-signal stability analysis of PLLs to predict their low-frequency unstable oscillations in grid-connected converter systems [18]. During the process of small-signal analysis, small-signal linearization methods and linear control theories are utilized to simplify the analysis [19]. For example, a unified small-signal impedance model of grid-connected voltage-source converters (VSCs) is established in [20], to predict the stability impact of the PLL. In [21], the linearized grid-synchronization loop and the self-synchronization loop are proposed to explain the interaction of the power grid and the injection current in a grid-connected VSC. However, the small-signal analysis can only predict the stability of PLLs around steady-states and cannot reflect the failure process and instability mechanism under grid faults.

To study the instability process of the PLL under faults, transient stability analysis is needed. Some literature uses power-angle curves or voltage-angle curves to describe the transient process of PLLs in different scenarios [19], [22]-[24]. In a grid-connected converter system without current limitation, phase-portrait analysis is adopted to study the transient responses of the converter with a power synchronization control [22], [23]. In a current limited grid-connected converter system, the converter reaching the current limitation can be regarded as a current source which is only controlled by the reference current. The dynamic behavior of PLLs in such situations has been analyzed in [19]. However, in this research, the control loops are simplified or ignored. In [25], a current loop with a voltage feedforward filter is adopted to prevent instability of the grid-connected system, but the dynamic responses of the PLL are ignored. In a previous work that considers both the control loop and the PLL [16], the response of the PLL influenced by the control loop is neglected. In practical grid-connected systems, the behaviors of PLLs may be influenced by the widely-used inner current loop and outer power/voltage loop. Hence, analyzing the transient stability of the PLL considering the influence of the dynamics of the control loop under grid faults is of great significance.

In this paper, the PLL affected by the current loop and the power loop in a grid-connected modular multilevel converter (MMC) is taken into consideration. The outline of this paper is

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arranged as follows. In Section II, the equivalent model of the PLL is established to present the interaction with the control loop. In Section III, the transient process of how the control loop influences the PLL under the ground fault is clarified. In Section IV, a small-signal analysis model is proposed to assess the stability of the PLL after a ground fault under different control loop parameters. In Section V, simulations of a grid-connected three-phase 21-level MMC built in PSCAD are performed to analyze the parameter influence and verify the analysis above. Section VI provides our conclusions.

II. EQUIVALENT MODEL OF PLL

In order to study the stability of the PLL influenced by the control loop under grid faults, a grid-connected MMC system disturbed by a grid ground fault is presented in this paper. The system is shown in Fig. 1. The AC grid is a non-ideal power grid, where $Z_{\rm g}$, $Z_{\rm line1}$ and $Z_{\rm line2}$ are the inner impedances of the AC grid. $Z_{\rm g}$ represents the equivalent impedance of series transmission lines in the power grid, while $Z_{\rm line1}$ and $Z_{\rm line2}$ represent the impedances of two paralleled transmission lines (line 1 and line 2). The MMC is connected to the AC grid at the point of common coupling (PCC), as shown in Fig. 1. $Z_{\rm f}$ is the impedance of the AC filter. $Z_{\rm gnd}$ is the ground impedance. The topology of the three-phase MMC is shown in Fig. 2.



Fig. 1. Grid-connected MMC system.



Fig. 2. Topology of three-phase MMC.

To analyze the stability of the PLL in the grid-connected three-phase MMC system under a grid fault, the phasor diagram is shown in Fig. 3. The black arrows represent the voltage vectors before the fault and the red arrows represent the voltage vectors after the fault. In the phasor diagram, it can be seen that the ground fault leads to a phase jump, since the grid impedance $Z_{\rm s}$ changes from $Z_{\rm s1}$ to $Z_{\rm s2}$, where $Z_{\rm s1} = Z_{\rm g} + (Z_{\rm line1} / / Z_{\rm line2})$ before the fault and $Z_{\rm s} = Z_{\rm s2} = Z_{\rm s1} / / Z_{\rm gnd}$ after the fault.



Fig. 3. Phasor diagram before and after fault.

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Before the fault, the voltage drop on the grid inductance $L_{\rm s1}$ can be ignored. Due to the effect of the PLL, the phase angle of the voltage at PCC $\theta_{\rm PCC}$, the output phase angle of the PLL $\theta_{\rm PLL}$ and the grid phase $\theta_{\rm g}$ can be regarded as the same, i.e., $\theta_{\rm PCC} = \theta_{\rm PLL} = \theta_{\rm g}$. Thus, the system operates with a unity power factor before the fault, in which case the voltage at PCC can be given as:

$$V_{\text{PCC}} \angle \theta_{\text{PCC}} = V_{\text{g}} \angle \theta_{\text{g}} + I_{\text{g}} Z_{\text{s1}} \angle \theta_{\text{g}}$$
(1)

However, when the fault happens, the grid impedance Z_s will become smaller (i.e. Z_{s2}), and the phase angle of the grid impedance θ_{s2} may change suddenly. The phases θ_{PCC} , θ_{PLL} and θ_g are unable to stay the same any more.

Figure 4 shows the Norton equivalent circuit of the AC grid after the ground fault. The amplitude of equivalent grid voltage would drop to $V_{g1} = V_g Z_{s2}/Z_{s1}$. Ignoring the phase variation of the equivalent grid voltage v_{g1} and assuming the grid current i_g remains unchanged, the amplitude of voltage at PCC V_{PCC} would decrease, as shown in Fig. 3. The PCC voltage in d-axis v_{PCCd} may decline with the drop of V_{PCC} , and the PCC voltage in q-axis v_{PCCq} may slightly increase with the growth of the phase angle θ_{PCC} . The PCC voltage at the moment of the fault happening can be calculated as:

$$V_{\text{PCC}} \angle \theta_{\text{PCC}} = V_{\text{g1}} \angle \theta_{\text{g}} + I_{\text{g}} Z_{\text{s2}} \angle (\theta_{\text{g}} + \theta_{\text{s2}})$$
(2)

$$V_{\text{g}} \angle \theta_{\text{g}} Z_{\text{s1}} + V_{\text{PCC}} \angle \theta_{\text{PCC}} + V_{\text{g1}} \angle \theta_{\text{g}} Z_{\text{s2}} + V_{\text{PCC}} \angle \theta_{\text{PCC}} + V_{\text{g1}} \angle \theta_{\text{g2}} Z_{\text{s2}} + V_{\text{PCC}} \angle \theta_{\text{PCC}} + V_{\text{g1}} \angle \theta_{\text{g2}} Z_{\text{s2}} + V_{\text{PCC}} \angle \theta_{\text{PCC}} + V_{\text{g1}} \angle \theta_{\text{g2}} Z_{\text{g1}} + V_{\text{g2}} Z_{\text{g1}} + V_{\text{g2}} Z_{\text{g1}} + V_{\text{g2}} Z_{\text{g1}} + V_{\text{g2}} Z_{\text{g2}} + V_{\text{g2}} +$$

Fig. 4. Norton equivalent circuit of the AC grid after ground fault.

After the fault, the PLL and the control loop work to adjust the operational state of the MMC system which is connected to a weak power grid. We can establish a two-source equivalent circuit of this grid-connected system after the fault as shown in Fig. 5.



Fig. 5. Two-source equivalent circuit.

Figure 5 shows that the voltage at PCC v_{PCC} is affected by both the equivalent grid voltage v_{g1} and the equivalent output voltage of the MMC e_v . Z_s and Z_{eq} represent the grid impedance and the equivalent impedance of the MMC respectively, where $Z_{eq} = Z_f + Z_0/2$. According to the twosource equivalent circuit of the MMC system, the voltage at PCC can be obtained as:

$$V_{PCC} \angle \theta_{PCC} = \frac{Z_{eq}(\omega_{g})}{Z_{s}(\omega_{g}) + Z_{eq}(\omega_{g})} V_{g1} \angle (\theta_{g} + \varphi_{1}) \\ + \frac{Z_{s}(\omega_{PLL})}{Z_{s}(\omega_{PLL}) + Z_{eq}(\omega_{PLL})} E_{v} \angle (\theta_{v} + \varphi_{2}) \quad (3)$$

$$\begin{cases} K_{1}(\omega) = \left| \frac{Z_{eq}(\omega)}{Z_{s}(\omega) + Z_{eq}(\omega)} \right| \\ K_{2}(\omega) = \left| \frac{Z_{s}(\omega)}{Z_{s}(\omega) + Z_{eq}(\omega)} \right| \\ K_{2}(\omega) = \left| \frac{Z_{eq}}{Z_{s}(\omega)} \right| \\ = \arctan \left(\frac{Z_{eq}}{Z_{s} + Z_{eq}} \right) \\ = \arctan \left(\frac{\omega L_{eq} R_{s} - \omega L_{s} R_{eq}}{R_{eq}(R_{eq} + R_{s}) + \omega^{2} L_{eq}(L_{eq} + L_{s})} \right) \end{cases} \quad (5)$$

$$\begin{pmatrix} \varphi_2 = \text{phase}\left(\frac{Z_s + Z_{eq}}{Z_s + Z_{eq}}\right) \\ = \arctan\frac{\omega L_s R_{eq} - \omega L_{eq} R_s}{R_s (R_{eq} + R_s) + \omega^2 L_s (L_{eq} + L_s)} \end{cases}$$

where $E_{\rm v}$ represents the amplitude of the MMC equivalent output voltage $e_{\rm v}$. $\omega_{\rm g}$ is the angular frequency of the power grid and $\omega_{\rm PLL}$ is the output angular frequency of the PLL.

Transforming v_{PCC} into dq rotating reference frame, the dq-axis voltage of v_{PCC} can be calculated as:

$$\begin{cases} v_{\text{PCCd}} = K_1(\omega_{\text{g}})V_{\text{g1}}\cos[\theta_{\text{g}} + \varphi_1(\omega_{\text{g}}) - \theta_{\text{PLL}}] \\ + K_2(\omega_{\text{PLL}})E_{\text{v}}(\omega_{\text{PLL}})\cos[\theta_{\text{v}} + \varphi_2(\omega_{\text{g}}) - \theta_{\text{PLL}}] \\ v_{\text{PCCq}} = K_1(\omega_{\text{g}})V_{\text{g1}}\sin[\theta_{\text{g}} + \varphi_1(\omega_{\text{g}}) - \theta_{\text{PLL}}] \\ + K_2(\omega_{\text{PLL}})E_{\text{v}}(\omega_{\text{PLL}})\sin[\theta_{\text{v}} + \varphi_2(\omega_{\text{g}}) - \theta_{\text{PLL}}] \end{cases}$$
(6)

Based on the control block of the PLL presented in Fig. 6, the output phase angle of the PLL is obtained from a PI and an integral process. Thus, the output phase angle can be written as:

$$\theta_{\rm PLL} = \int [\omega_{\rm g} + (K_p + K_i f) v_{\rm PCCq}]$$
(7)



Fig. 6. Control diagram of PLL.

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Substituting (6) into (7), the control equation of the PLL can be rewritten as:

$$\theta_{\text{PLL}} = \int \{ \omega_{\text{g}} + (K_p + K_i \int) [K_1 V_{\text{g1}} \sin(\theta_{\text{g}} + \varphi_1 - \theta_{\text{PLL}}) + K_2 E_{\text{v}} \sin(\theta_{\text{v}} + \varphi_2 - \theta_{\text{PLL}})] \}$$
(8)

Since the phase angle of the equivalent output voltage θ_v is provided by the PLL, θ_v is regarded as equal to θ_{PLL} in this

paper. Considering the voltage drop on the impedance $I_g Z_s$ is far smaller than the equivalent grid voltage v_{g1} , the phase angle of the PCC voltage θ_{PCC} can be regarded as equal to the grid phase θ_g , i.e., $\theta_{PCC} \approx \theta_g$. Define the phase angle difference between θ_{PLL} and θ_{PCC} as δ , there is:

$$\delta = \theta_{\rm PCC} - \theta_{\rm PLL} \approx \theta_{\rm g} - \theta_{\rm PLL} \tag{9}$$

Thus, the equivalent model of the PLL can be expressed as:

$$\delta = \int \{ (K_p + K_i f) [K_1 V_{g1} \sin(\varphi_1 + \delta) + K_2 E_v \sin \varphi_2] \}$$
(10)

which reflects the PLL behavior under the influence of the grid impedance and the output voltage of the control loop. Based on (10), the control block of the PLL considering the interaction of the control loop after the grid fault can be plotted, as shown in Fig. 7.



Fig. 7. Control diagram of PLL with the interaction of the control loop.

Assuming that the equivalent output voltage of the MMC is equal to the output command of the control loop, i.e., $e_v \approx e_v^*$, the red part in Fig. 7 represents the effect of the control loop on the PLL. Actually, in many researchers' previous works, the output voltage or current of the converter is always given as a constant, which may not be disturbed by the grid fault and cannot reflect the influence of the control loop. However, in this paper, the variation of E_v after the fault, which shows the dynamic of the control loop, is considered.

III. INFLUENCE OF CONTROL LOOP

From the analysis in Section II, it can be shown that the d-axis voltage v_{PCCd} would decrease and the q-axis voltage v_{PCCq} slightly increase when a ground fault happens in line2, which will lead to the increasing of $\dot{\delta}$ and δ . The variation of v_{PCCd} and v_{PCCq} will also cause the action of both the inner current loop and outer power loop.

According to the control diagram of the outer voltage loop in Fig. 8, the control equation is given as:

$$\begin{cases} i_{\text{dref}} = (K_{p2} + K_{i2} \int) \left(P_{\text{ref}} - \frac{3}{2} i_{\text{d}} v_{\text{PCCd}} - \frac{3}{2} i_{\text{q}} v_{\text{PCCq}} \right) \\ i_{\text{qref}} = (K_{p2} + K_{i2} \int) \left(Q_{\text{ref}} - \frac{3}{2} i_{\text{q}} v_{\text{PCCd}} + \frac{3}{2} i_{\text{d}} v_{\text{PCCq}} \right) \end{cases}$$
(11)

where K_{p2} and K_{i2} are the proportional gain and integral gain of the power loop.

$$\begin{array}{c} \underline{P_{\text{ref}}} & & \\ + & \\ + & \\ \end{array} \end{array} \xrightarrow{P} & PI \\ \hline \\ \underline{Q_{\text{ref}}} & \\ + & \\ - & \underline{Q} \\ \end{array} \xrightarrow{PI \\ } \begin{array}{c} i_{\text{dref}} \\ i_{\text{qref}} \\ \end{array} \xrightarrow{i_{\text{qref}}} \end{array}$$

Fig. 8. Outer power loop.

In (11), the decrease of v_{PCCd} from its steady value indicates the power loss in the AC side of the MMC. Thus, the reference value of d-aixs current i_{dref} may show an increasing trend under the grid ground fault, and i_{qref} cannot stay at zero.

When the reference currents vary, the output voltage commands may be changed due to the action of the inner current loop. From the inner current loop shown in Fig. 9, the dq-axis output voltage commands e_{vd}^* and e_{vq}^* can be given by the control equation of the current loop as follows:

$$\begin{cases} e_{\mathrm{vd}}^* = v_{\mathrm{PCCd}} + \omega L_{\mathrm{eq}} i_{\mathrm{q}} + (K_{p1} + K_{i1} \int) (i_{\mathrm{dref}} - i_{\mathrm{d}}) \\ e_{\mathrm{vq}}^* = v_{\mathrm{PCCq}} - \omega L_{\mathrm{eq}} i_{\mathrm{d}} + (K_{p1} + K_{i1} \int) (i_{\mathrm{qref}} - i_{\mathrm{q}}) \end{cases}$$
(12)

where K_{p1} and K_{i1} are the proportional gain and the integral gain of the current loop. The amplitude of the equivalent output voltage E_v that transfers the influence of the control loop to the PLL can be given as:

$$E_{\rm v} \approx E_{\rm v}^* = \sqrt{e_{\rm vd}^{*2} + e_{\rm vq}^{*2}}$$
 (13)

where E_v^* is the amplitude of the output voltage commands e_v^* . Since the voltage commands in q axis e_{vq}^* varies around zero and the voltage commands in d axis e_{vd}^* is much higher than e_{vq}^* , the variation trend of E_v^* is primarily determined by e_{vd}^* .



Fig. 9. Inner current loop.

From (12), it can be seen that the variation of the voltage commands e_{vd}^* are primarily affected by v_{PCCd} and i_{dref} . Thus, analyzing whether v_{PCCd} or i_{dref} determine the variation trend of e_{vd}^* is essential. The dominant factor of the variation trend of e_{vd}^* may be related to the control parameters of the inner current loop, such as the proportional gain K_{p1} .

When there is a smaller K_{p1} in the current loop, e_{vd}^* may decline with the decrease of v_{PCCd} . Thus, the amplitude of the output voltage E_v may drop to a smaller value according to equation (13). Since φ_1 and φ_2 have opposite signs according to equation (5), we can suppose that the sign of φ_1 is positive as an example. Under this assumption, $\sin \varphi_2$ in Fig. 8 is a negative value, the q-axis voltage at PCC $K_1V_{g1}\sin(\varphi_1+\delta) +$ $K_2E_v\sin\varphi_2$ may show an increasing tendency. The control loop and the PLL may form a positive feedback. The phase angle difference δ will continue to grow and diverge to infinity, in which case the PLL will become unstable.

When there is a larger K_{p1} in the current loop, e_{vd}^* may become higher with the increase of i_{dref} . The amplitude of the output voltage E_v may rise accordingly. With a negative $\sin \varphi_2$ in Fig. 8, $K_1V_{g1}\sin(\varphi_1 + \delta) + K_2E_v\sin\varphi_2$ may decline. The control loop and the PLL may form a negative feedback. The phase angle difference δ will show a convergent tendency and recover to its steady value, in which case the PLL can keep stable.

Similarly, the outer power control loop affects the responses of the PLL by changing the variation trend of $e_{\rm vd}^*$. When there is a larger proportional gain of the power loop K_{p2} , the system will become more stable. As the d-axis voltage v_{PCCd} decreases because of the phase disturbance, the d-axis reference current i_{dref} will increase. The value of K_{p2} will determine the growth degree of i_{dref} as shown in (11). If there is a larger K_{p2} , i_{dref} will grow more, which causes e_{yd}^* to have an increasing tendency. Then, the control loop and the PLL will form a negative feedback, and the system can recover to a stable state. However, if there is a smaller K_{p2} , the increase of i_{dref} may be slight, and the variation tendency of e_{vd}^* is determined by the drop of v_{PCCd} . Thus, in this situation, the control loop and the PLL may form a positive feedback, and cannot remain stable anymore. The response processes of the PLL with the interaction of the control loop under grid fault are presented in Fig. 10.



Fig. 10. Response process of PLL with interaction of the control loop under grid fault.

IV. SMALL-SIGNAL STABILITY ANALYSIS OF PLL Considering The Interaction with THE Control Loop

From the qualitative analysis above, how the gains of both the current loop and the power loop affect the stability of the PLL is clarified by the block diagram in Fig. 10. However, to analyze the parameter influence of the system with exact values, a quantitative calculation is needed. In this section, a small-signal model of the PLL considering the interaction of the control loop is established to analyze the small-signal stability and the parameter influence of the PLL after the fault.

According to (6), the linearized small-signal model can be obtained around the steady-state operating point, i.e., $\omega = \omega_g$.

Since the phase angle of the equivalent output voltage θ_v is provided by the PLL, θ_v is regarded as equal to θ_{PLL} in this paper. Considering the PLL is able to follow the grid phase angle when the system operates in a stable state, the small-

signal equation of (6) can be written as:

$$\begin{cases} \Delta v_{\text{PCCd}} = G_1(\Delta \theta_{\text{g}} - \Delta \theta_{\text{PLL}}) + G_2 \Delta \omega + G_3 \Delta E_{\text{v}} \\ \Delta v_{\text{PCCq}} = G_4(\Delta \theta_{\text{g}} - \Delta \theta_{\text{PLL}}) + G_5 \Delta \omega + G_6 \Delta E_{\text{v}} \end{cases}$$
(14)

where

$$\begin{cases}
G_{1} = -K_{1}(\omega_{g})V_{g1}\sin[\varphi_{1}(\omega_{g})] \\
G_{2} = \{-K_{2}(\omega_{g})\sin[\varphi_{2}(\omega_{g})]\varphi'_{2}(\omega_{g}) \\
+ K'_{2}(\omega_{g})\cos[\varphi_{2}(\omega_{g})]\}E_{v}(\omega_{g}) \\
G_{3} = K_{2}(\omega_{g})\cos[\varphi_{2}(\omega_{g})] \\
G_{4} = K_{1}(\omega_{g})V_{g1}\cos[\varphi_{1}(\omega_{g})] \\
G_{5} = \{K_{2}(\omega_{g})\cos[\varphi_{2}(\omega_{g})]\varphi'_{2}(\omega_{g}) \\
+ K'_{2}(\omega_{g})\sin[\varphi_{2}(\omega_{g})]\}E_{v}(\omega_{g}) \\
G_{6} = K_{2}(\omega_{g})\sin[\varphi_{2}(\omega_{g})]
\end{cases}$$
(15)

In (14), $\Delta E_{\rm v}$ is the small-signal increment of $E_{\rm v}$, and $E_{\rm v}(\omega_{\rm g})$ is the steady-state value of $E_{\rm v}$ when the angular frequency keeps stable at $\omega_{\rm g}$. In previous studies [18], the output voltage or current of the converter is regarded as the same as the reference values, without considering the dynamic behaviors of the control loop. However, the dynamic of the control loop is taken into consideration in this paper. The calculation of $\Delta E_{\rm v}$ will reflect the action of the control loop under the phase disturbance, so it is quite essential to derive the small-signal increment $\Delta E_{\rm v}$.

The small-signal linearized expression of E_v can be obtained from (13) when the system operates around the steady-state point ω_g , i.e.,

$$\Delta E_{\rm v} \approx [e_{\rm vd}^*(\omega_{\rm g}) + e_{\rm vq}^*(\omega_{\rm g})](\Delta e_{\rm vd}^* + \Delta e_{\rm vq}^*)/E_{\rm v}(\omega_{\rm g}) \quad (16)$$

According to the control equation of the current loop (12), the small-signal items $\Delta e_{\rm vd}^*$ and $\Delta e_{\rm vq}^*$ in (16) can be expressed as the linearized inner current control in (17).

$$\begin{cases}
\Delta e_{\rm vd}^* = \Delta v_{\rm PCCd} + L_{\rm eq} I_{\rm q} \Delta \omega + \omega_{\rm g} L_{\rm eq} \Delta i_{\rm q} \\
+ G_i (\Delta i_{\rm dref} - \Delta i_{\rm d}) \\
\Delta e_{\rm vq}^* = \Delta v_{\rm PCCq} - L_{\rm eq} I_{\rm d} \Delta \omega - \omega_{\rm g} L_{\rm eq} \Delta i_{\rm d} \\
+ G_i (\Delta i_{\rm qref} - \Delta i_{\rm q})
\end{cases}$$
(17)

where $G_i = K_{p1} + K_{i1}$ /s.

Similarly, the dq-axis reference current increment Δi_{dref} and Δi_{qref} can be given from the control equation of the power loop (11), i.e.,

$$\begin{cases} \Delta i_{\text{dref}} = \frac{3}{2} G_p (-I_{\text{d}} \Delta v_{\text{PCCd}} - V_{\text{PCCd}} \Delta i_{\text{d}} \\ -I_{\text{q}} \Delta v_{\text{PCC}} q - V_{\text{PCCq}} \Delta i_{\text{q}}) \\ \Delta i_{\text{qref}} = \frac{3}{2} G_p (-I_{\text{q}} \Delta v_{\text{PCCd}} - V_{\text{PCCd}} \Delta i_{\text{q}} \\ +I_{\text{d}} \Delta v_{\text{PCC}} q + V_{\text{PCC}} q \Delta i_{\text{d}}) \end{cases}$$
(18)

where $G_p = K_{p2} + K_{i2}/s$.

Combining (16), (17) and (18), the small-signal increment of $E_{\rm v}$ can be derived as:

$$\Delta E_{\rm v} \approx J_1 \Delta v_{\rm PCCd} + J_2 \Delta v_{\rm PCCq} + J_3 \Delta i_{\rm d} + J_4 \Delta i_{\rm q} + J_5 \Delta \omega$$
(19)

where

$$\begin{cases} J_{1} = \left(1 - \frac{3}{2}G_{i}G_{p}I_{d} - \frac{3}{2}G_{i}G_{p}I_{q}\right) [e_{vd}^{*}(\omega_{g}) \\ + e_{vq}^{*}(\omega_{g})]/E_{v}(\omega_{g}) \\ J_{2} = \left(1 + \frac{3}{2}G_{i}G_{p}I_{d} - \frac{3}{2}G_{i}G_{p}I_{q}\right) [e_{vd}^{*}(\omega_{g}) \\ + e_{vq}^{*}(\omega_{g})]/E_{v}(\omega_{g}) \\ J_{3} = \left(\frac{3}{2}G_{i}G_{p}V_{PCCq} - \frac{3}{2}G_{i}G_{p}V_{PCCd} - G_{i} - \omega_{g}L_{eq}\right) (20) \\ [e_{vd}^{*}(\omega_{g}) + e_{vq}^{*}(\omega_{g})]/E_{v}(\omega_{g}) \\ J_{4} = \left(\omega_{g}L_{eq} - \frac{3}{2}G_{i}G_{p}V_{PCCq} - \frac{3}{2}G_{i}G_{p}V_{PCCd} - G_{i}\right) \\ [e_{vd}^{*}(\omega_{g}) + e_{vq}^{*}(\omega_{g})]/E_{v}(\omega_{g}) \\ J_{5} = L_{eq}(I_{q} - I_{d})[e_{vd}^{*}(\omega_{g}) + e_{vq}^{*}(\omega_{g})]/E_{v}(\omega_{g}) \end{cases}$$

Considering the relationship of the grid voltage and current in Fig. 5, the grid voltage and current should satisfy the following equation:

$$I_{g} \angle \theta_{i} = \frac{1}{Z_{s}(\omega_{PLL}) + Z_{eq}(\omega_{PLL})} E_{v} \angle \theta_{v}$$
$$- \frac{1}{Z_{s}(\omega_{g}) + Z_{eq}(\omega_{g})} V_{g1} \angle \theta_{g}$$
$$= K_{3}(\omega_{PLL}) E_{v} e^{j[\theta_{v} + \varphi_{3}(\omega_{PLL})]}$$
$$- K_{3}(\omega_{g}) V_{g1} e^{j[\theta_{g} + \varphi_{3}(\omega_{g})]}$$
(21)

where

$$\begin{split} K_{3}(\omega) &= \frac{1}{|Z_{\rm s}(\omega) + Z_{\rm eq}(\omega)|},\\ \varphi_{3}(\omega) &= {\rm phase}\left(\frac{1}{Z_{\rm s}(\omega) + Z_{\rm eq}(\omega)}\right) \end{split}$$

Thus, $\Delta i_{\rm d}$ and $\Delta i_{\rm q}$ in (19) can be given as:

$$\begin{cases} \Delta i_{\rm d} = H_1 \Delta \omega + H_2 \Delta e_{vm} + H_3 (\Delta \theta_{\rm g} - \Delta \theta_{\rm PLL}) \\ \Delta i_{\rm q} = H_4 \Delta \omega + H_5 \Delta e_{vm} + H_6 (\Delta \theta_{\rm g} - \Delta \theta_{\rm PLL}) \end{cases}$$
(22)

where

$$\begin{cases}
H_{1} = K'_{3}(\omega_{g})E_{v}(\omega_{g})\cos[\varphi_{3}(\omega_{g})] \\
-K_{3}E_{v}(\omega_{g})\varphi'_{3}(\omega_{g})\sin[\varphi_{3}(\omega_{g})] \\
H_{2} = K_{3}(\omega_{g})\cos[\varphi_{3}(\omega_{g})] \\
H_{3} = K_{3}(\omega_{g})V_{g1}\sin[\varphi_{3}(\omega_{g})] \\
H_{4} = K'_{3}(\omega_{g})E_{v}(\omega_{g})\sin[\varphi_{3}(\omega_{g})] \\
+K_{3}(\omega_{g})E_{v}(\omega_{g})\varphi'_{3}(\omega_{g})\cos[\varphi_{3}(\omega_{g})] \\
H_{5} = K_{3}(\omega_{g})\sin[\varphi_{3}(\omega_{g})] \\
H_{6} = -K_{3}(\omega_{g})V_{g1}\cos[\varphi_{3}(\omega_{g})]
\end{cases}$$
(23)

Combining (22) and (19), there is:

$$\Delta E_{\rm v} = \frac{J_3 H_1 + J_4 H_4 + J_5}{1 - J_3 H_2 - J_4 H_5} \Delta \omega + \frac{J_1}{1 - J_3 H_2 - J_4 H_5} \Delta v_{\rm PCCd} + \frac{J_2}{1 - J_3 H_2 - J_4 H_5} \Delta v_{\rm PCCq} + \frac{J_3 H_3 + J_4 H_6}{1 - J_3 H_2 - J_4 H_5} (\Delta \theta_{\rm g} - \Delta \theta_{\rm PLL}) = T_1 \Delta \omega + T_2 \Delta v_{\rm PCCd} + T_3 \Delta v_{\rm PCCq} + T_4 (\Delta \theta_{\rm g} - \Delta \theta_{\rm PLL})$$
(24)

And then substituting (24) into (14), Δv_{PCCq} can be rewritten with only three small-signal items that are related to frequency and angle, i.e., $\Delta \omega$, $\Delta \theta_g$ and $\Delta \theta_{PLL}$, as shown in (25).

$$\Delta v_{\rm PCCq} = F_1 \Delta \omega + F_2 (\Delta \theta_{\rm g} - \Delta \theta_{\rm PLL}) \tag{25}$$

where

$$\begin{cases} F_1 = \frac{(G_5 + G_6 T_1)(1 - G_3 T_2) + G_6 T_2 (G_2 + G_3 T_1)}{(1 - G_3 T_2)(1 - G_6 T_3) - G_6 T_2 G_3 T_3} \\ F_2 = \frac{(G_4 + G_6 T_4)(1 - G_3 T_2) + G_6 T_2 (G_1 + G_3 T_4)}{(1 - G_3 T_2)(1 - G_6 T_3) - G_6 T_2 G_3 T_3} \end{cases}$$
(26)

Then, the small-signal model of the PLL in the gridconnected MMC system can be established in (27) and the model around the operating point can be also described in Fig. 11. The red part of Fig. 11 shows the influence of the control loop on the PLL. In Fig. 11, the interaction between the PLL and the control loop is presented clearly. The control loop affects the PLL by changing the output voltage of the MMC $\Delta E_{\rm v}$, and the output phase $\Delta \theta_{\rm PLL}$ and angular frequency $\Delta \omega$ of the PLL will further affect the output voltage of the control loop $\Delta E_{\rm v}$.

$$\Delta \theta_{\text{PLL}} = [F_1 \Delta \omega + F_2 (\Delta \theta_{\text{g}} - \Delta \theta_{\text{PLL}})] \left(K_p + \frac{K_i}{s} \right) \frac{1}{s} \quad (27)$$



Fig. 11. Small-signal model of PLL.

According to (27), the input and output transfer function of the PLL can be derived as follows:

$$\frac{\Delta\theta_{\rm PLL}}{\Delta\theta_{\rm g}} = \frac{K_p F_2 s + K_i F_2}{(1 - K_p F_1) s^2 + (K_p F_2 - K_i F_1) s + K_i F_2} = \frac{N(s)}{D(s)}$$
(28)

Solving the poles of the transfer function (28), the stability of the PLL can be assessed by analyzing the sign of the real parts of the poles. When there is no pole in the right half-plane, the PLL can remain stable after the fault. On the contrary, if there is any pole staying in the right half-plane, the PLL will lose stability.

V. VERIFICATION

In this section, a grid-connected three-phase 21-level MMC simulation model is built in the PSCAD platform to verify the analysis of the response process in Fig. 10. The simulation model is shown in Fig. 1 and Fig. 2, and the parameters of the grid-connected MMC system are listed in Table I.

TABLE I Parameters of Grid-connected MMC system

| System parameter | Value |
|--|----------|
| AC voltage $v_{\rm g}$ (kV) | 23 |
| Phase of AC voltage θ_{g} (deg) | 0 |
| Rated DC voltage V_{dc} (kV) | 40 |
| Number of SMs per arm N | 20 |
| SM capacitance \overline{C} (mF) | 10 |
| Reference value of active power P_{ref} (MW) | 40 |
| Reference value of reactive power Q_{ref} (MVar) | 0 |
| Proportional gain of PLL K_p | 0.2 |
| Integral gain of PLL K_i | 100 |
| AC grid frequency $f_{\rm g}$ (Hz) | 50 |
| Arm impedance $Z_0(L_0, R_0)$ (mH, Ω) | 16, 0.18 |
| AC filter impedance $Z_{\rm f}(L_{\rm f}, R_{\rm f})$ (mH, Ω) | 0.1, 0.1 |
| Series impedance $Z_{\rm g}(L_{\rm g}, R_{\rm g})$ (mH, Ω) | 0.1, 0.2 |
| Impedance of line 1 $Z_{\text{line1}}(L_{\text{line1}}, R_{\text{line1}})$ (mH, Ω) | 13, 0.2 |
| Impedance of line 2 $Z_{\text{line2}}(L_{\text{line2}}, R_{\text{line2}})$ (mH, Ω) | 29, 0.2 |
| Ground impedance $Z_{\text{gnd}}(L_{\text{gnd}}, R_{\text{gnd}})$ (mH, Ω) | 25, 0.1 |

In the MMC system, when a ground fault occurs in line 2, the grid impedance $Z_{\rm s}$ changes from $Z_{\rm g} + (Z_{\rm line1}//Z_{\rm line2})$ to $(Z_{\rm g} + (Z_{\rm line1}//Z_{\rm line2}))//Z_{\rm gnd}$. The equivalent grid voltage changes from $v_{\rm g}$ to $v_{\rm g1}$. The amplitude and the phase of the voltage at PCC may change accordingly, and then induce some dynamic behaviors of the PLL. To analyze the transient responses of the PLL influenced by the control loop under the ground fault, simulations with different control parameters are presented in this section.

A. Parameter Influence of K_{p1}

Figure 12 and Fig. 13 show the transient responses of the grid-connected MMC when the ground fault happens at 6 s with different proportional gains of the current loop K_{p1} .

When $K_{p1} = 10$, $K_{i1} = 0.5$, the system presents an abnormal operating state, as shown in Fig. 12. A divergent oscillation can be observed in the output angular frequency of the PLL. The active power shows a slight decrease and then recovers to its steady value. The reactive power, dqaxis voltage and current also oscillate and diverge with the divergency of the PLL output angular frequency. The AC voltage at PCC and AC grid current shows distortion due to the oscillations in the dq-axis voltage and current after the ground fault, which can be shown by the waveforms v_{PCCa} and i_{ga} in Fig. 12 (e)–(f). The waveforms in Fig. 12 verify the analysis that the PLL may lose stability after the fault with a smaller K_{p1} .

When $K_{p1} = 45$, $K_{i1} = 0.5$, the system presents a tendency to recover to a stable state, as shown in Fig. 13. From Fig. 13 (a), it can be seen that the output angular frequency of the PLL starts to oscillate after the fault, but the amplitude of the oscillation is within \pm 20 rad/s and shows a convergent trend. In Fig. 13 (b), the active power drops slightly and then recovers to its steady state, and the reactive power shows a slight oscillation. Fig. 13 (c) and (d) present the dq-axis voltage and current. The d-axis voltage at PCC decreases to 12.7 kV because of the grid fault, while the d-axis current increases to 2 kA. The q-axis voltage and current still stay at zero accompanied with slight convergent oscillations, which almost have no influence on the AC voltage at PCC v_{PCCa} and AC grid current waveforms i_{ga} , as shown in Fig. 13 (e)–



Fig. 12. Unstable transient responses of MMC when $K_{p1} = 10$. (a) Output angular frequency of PLL. (b) Active power/reactive power. (c) dq-axis voltage at PCC. (d) dq-axis grid current. (e) PCC voltage in phase *a*. (f) Grid current in phase *a*.



Fig. 13. Stable transient responses of MMC when $K_{p1} = 45$. (a) Output angular frequency of PLL. (b) Active power/reactive power. (c) dq-axis voltage at PCC. (d) dq-axis grid current. (e) PCC voltage in phase *a*. (f) Grid current in phase *a*.

(f). The waveforms in Fig. 13 verify the analysis that the PLL is able to remain stable after the fault when there is a larger K_{p1} .

Comparing the above two responses, the stability of the PLL

under the grid fault is changed due to the variation of the current loop proportional gain. From the simulation results, it can be shown that a larger proportional gain of the inner current loop may improve the stability of the PLL in a gridconnected MMC system under grid faults.

B. Parameter Influence of K_{p2}

Figure 14 shows the waveform of the MMC system when the proportional gain of the outer power loop K_{p2} is set as 5, and other parameters are the same as the parameters in Fig. 12, where $K_{p2} = 0.5$. Thus, the comparison of Fig. 14 and Fig. 12 can show the parameter influence of the outer power loop. As shown in Fig. 14, there are convergent oscillations in the waveforms of the output angular frequency of the PLL, the reactive power, the q-axis voltage and the q-axis current. Thus, it can be shown that the PLL has a tendency of recovering to a stable state with a larger K_{p2} .



Fig. 14. Stable transient responses of MMC when $K_{p2} = 5$. (a) Output angular frequency of PLL. (b) Active power/reactive power. (c) dq-axis voltage at PCC. (d) dq-axis grid current. (e) PCC voltage in phase *a*. (f) Grid current in phase *a*.

C. Parameter Influence of K_p

As the proportional gain of the PLL K_p is a quite essential parameter that has a great impact on the stability of the PLL, the influence of parameter K_p is also analyzed in this section.

When the proportional gain K_p decreases to 0.18 and the integral gain K_i remains unchanged at 100, the response waveforms of the grid-connected MMC under the ground fault with different current loop gains K_{p1} are presented in Fig. 15 and Fig. 16.

Figure 15 shows the transient responses of the MMC with the same current loop parameters as Fig. 13, i.e., $K_{p1} = 45$, $K_{i1} = 0.5$. With a smaller proportional gain K_p , the PLL cannot remain stable. The waveforms of the PLL output angular frequency, the reactive power, the q-axis voltage component



Fig. 15. Unstable transient responses of MMC when $K_{p1} = 45$. (a) Output angular frequency of PLL. (b) Active power/reactive power. (c) dq-axis voltage at PCC. (d) dq-axis grid current. (e) PCC voltage in phase *a*. (f) Grid current in phase *a*.



Fig. 16. Stable transient responses of MMC when $K_{p1} = 55$. (a) Output angular frequency of PLL. (b) Active power/reactive power. (c) dq-axis voltage at PCC. (d) dq-axis grid current. (e) PCC voltage in phase *a*. (f) Grid current in phase *a*.

and the q-axis current component present divergent tendencies when the ground fault occurs, as shown in Fig. 15 (a)–(d). Due to the divergent oscillations, there will be waveform distortion in the PCC voltage and the grid current, as shown in Fig. 15 (e)–(f).

According to the parameter analysis of the current loop proportional gain K_{p1} , it can be shown that the increase of

the current loop gain K_{p1} is able to improve the stability of the PLL. In Fig. 16, a larger current loop gain K_{p1} is set in the MMC system, where $K_{p1} = 55$ and $K_{i1} = 0.5$. Under this parameter condition, convergent oscillations can be seen in the PLL output angular frequency, the reactive power, the q-axis voltage and current components, which means that the MMC system is able to recover to a steady state and these oscillations will disappear after a finite time.

From the transient responses under a decreased proportional gain K_p , it can be concluded that a smaller K_p may have an adverse influence on the stability of the PLL. In addition, the critical value of K_{p1} in this MMC system will become larger when the proportional gain K_p declines. Thus, with a smaller PLL gain K_p , a larger current loop gain K_{p1} is needed to improve the stability of the PLL.

D. Verification of Small-signal Stability Analysis

Figure 17 present the pole-zero analysis results of the transfer function (24) when the system operates within the parameters in Fig. 12 and Fig. 13. When $K_{p1} = 10$, the pole-zero map can be seen in Fig. 17 (a). There is a pair of poles p_3 and p_4 in the right half plane, which means that PLL loses its stability. The stability analysis results and the simulation results shown in Fig. 12 match well. When $K_{p1} = 45$, all the poles are at the left half plane, confirming that the PLL can remain stable under such parameters. The pole-zero mapping of the transfer function is also in agreement with the simulation results shown in Fig. 13.



Fig. 17. Simulation results and pole-zero maps of the PLL under phase disturbance. (a) Pole-zero map of the small-signal model when $K_{p1} = 10$. (b) Pole-zero map of the small-signal model when $K_{p1} = 45$.

From Fig. 17, the effectiveness of the small-signal model and the stability analysis method presented in Section IV is verified, which also illustrates that the small-signal stability of the PLL can be affected by the parameter of the control loop. With the increase of the proportional gain K_{p1} , a pair of poles may cross the imaginary axis to the right half plane. Thus, the

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PLL can be more stable with a higher proportional gain of the current control loop. The stability analysis of the small-signal model can be used in the parameter design of grid-connected systems.

E. Experimental Verification

To further verify the analysis of the control loop's parameter influence on the PLL, down-scale hardware-in-the-loop (HIL) experiments with a two-level voltage-source inverter are performed in this section. The topology of the threephase voltage-source inverter is shown in Fig. 18. And the circuit parameters are listed in Table II. The circuit of the three-phase voltage-source inverter is established in the RT-LAB platform and the control part is achieved by a practical controller (STM32F401) with a FPGA (EP4CE115F23C7).

 TABLE II

 PARAMETERS OF TWO-LEVEL VOLTAGE-SOURCE INVERTER

| Parameter | Value | Parameter | Value |
|-------------------|-----------------|---------------------|---------------------|
| $V_{\rm dc}$ | 40 kV | $Z_{\rm g}$ | 0.1 mH, 0.2 Ω |
| $R_{ m dc}$ | $0.01 \ \Omega$ | $Z_{\rm ac}$ | 2 mH, 1 Ω |
| C | 16 mF | $Z_{\text{line 1}}$ | 13 mH, 0.2 Ω |
| $v_{ m g}$ | 23 kV | $Z_{\text{line}2}$ | 18 mH, 2 Ω |
| $\tilde{K_p}/K_i$ | 0.01/2 | $Z_{\rm gnd}$ | 29 mH, 0.1 Ω |



Fig. 18. Topology of the three-phase voltage-source inverter.

The HIL experimental results of PLL's output angular frequency with different control parameters are presented in Fig. 19. The output angular frequency of the PLL diverges



Fig. 19. Experimental results of PLL's output angular frequency with different control loop parameters. (a) Unstable response when $K_{p1} = 1.8$. (b) Stable response when $K_{p1} = 2.4$.

as soon as grid fault occurs when $K_{p1} = 1.8$, as shown in Fig. 19 (a). However, when there is a larger K_{p1} , i.e., $K_{p1} = 2.4$, the output angular frequency recovers to the steady-state operating point ($\omega_{PLL} = \omega_g = 314$ rad/s) as shown in Fig. 19 (b). From the experimental results, the theory analysis of the PLL influenced by the dynamics of the control loop can be further validated.

VI. CONCLUSION

In the practical grid-connected power electronics converter system, the responses of PLL are not only determined by their own parameters, but are also related to the control loops. In this study, the post fault response process of the PLL considering the influence of the control loop is investigated in a grid-connected MMC system. By establishing the equivalent model of the PLL with the interaction of the control loop, the influence of the control loop on the behaviors of the PLL can be analyzed. A small-signal model and the corresponding pole-zero map are proposed to provide a qualitative stability assessment. It is shown that when the control loops have a lower proportional gain and form a positive feedback with the PLL under a certain parameter condition, the system will lose stability. It can be concluded that the stability of the PLL can be influenced by the dynamics of the control loop, and destabilized by the grid-connected system during a transient fault.

REFERENCES

- L. B. Huang, H. H. Xin, and Z. Wang, "Damping low-frequency oscillations through VSC-HVDC stations operated as virtual synchronous machines," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5803–5818, Jun. 2019.
- [2] W. J. Du, Q. Fu, and H. F. Wang, "Power system small-signal angular stability affected by virtual synchronous generators," *IEEE Transactions* on *Power Systems*, vol. 34, no. 4, pp. 3209–3219, Jul. 2019.
- [3] E. Ebrahimzadeh, F. Blaabjerg, X. F. Wang, and C. L. Bak, "Optimum design of power converter current controllers in large-scale power electronics based power systems," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2792–2799, May/Jun. 2019.
- [4] W. Dong, H. H. Xin, D. Wu, and L. B. Huang, "Small signal stability analysis of multi-infeed power electronic systems based on grid strength assessment," *IEEE Transactions on Power Systems*, vol. 34, no. 2, pp. 1393–1403, Mar. 2019.
- [5] X. F. Wang and F. Blaabjerg, "Harmonic stability in power electronicbased power systems: concept, modeling, and analysis," *IEEE Transactions on Smart Grid*, vol. 10, no. 3, pp. 2858–2870, May 2019.
- [6] A. Bidadfar, H. P. Nee, L. D. Zhang, L. Harnefors, S. Namayantavana, M. Abedi, M. Karrari, and G. B. Gharehpetian, "Power system stability analysis using feedback control system modeling including hvdc transmission links," *IEEE Transactions on Power Systems*, vol. 31, no. 1, pp. 116–124, Jan. 2016.
- [7] B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Y. Shen, "Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 26–38, Jan. 2016.
- [8] Y. F. Wen, J. P. Zhan, C. Y. Chung, and W. Y. Li, "Frequency stability enhancement of integrated AC/VSC-MTDC systems with massive infeed of offshore wind generation," *IEEE Transactions on Power Systems*, vol. 33, no. 5, pp. 5135–5146, Sep. 2018.
- [9] F. Nejabatkhah, Y. W. Li, K. Sun, and R. X. Zhang, "Active power oscillation cancelation with peak current sharing in parallel interfacing converters under unbalanced voltage," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10200–10214, Dec. 2018.
- [10] A. A. A. Radwan and Y. A. R. I. Mohamed, "Improved vector control strategy for current-source converters connected to very weak grids," *IEEE Transactions on Power Systems*, vol. 31, no. 4, pp. 3238–3248, Jul. 2016.

- [11] I. Carugati, P. Donato, S. Maestri, D. Carrica, and M. Benedetti, "Frequency adaptive PLL for polluted single-phase grids," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2396–2404, May 2012.
- [12] M. G. Taul, X. F. Wang, P. Davari, and F. Blaabjerg, "An overview of assessment methods for synchronization stability of grid-connected converters under severe symmetrical grid faults," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9655–9670, Oct. 2019.
- [13] M. Huang, Y. Peng, C. K. Tse, Y. S. Liu, J. J. Sun, and X. M. Zha, "Bifurcation and large-signal stability analysis of three-phase voltage source converter under grid voltage dips," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8868–8879, Nov. 2017.
- [14] S. Mortazavian, M. M. Shabestary, and Y. A. R. I. Mohamed, "Analysis and dynamic performance improvement of grid-connected voltage– source converters under unbalanced network conditions," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 8134–8149, Oct. 2017.
- [15] Q. Hu, L. J. Fu, F. Ma, and F. Ji, "Large signal synchronizing instability of PLL-based VSC connected to weak AC grid," *IEEE Transactions on Power Systems*, vol. 34, no. 4, pp. 3220–3229, Jul. 2019.
- [16] M. G. Taul, X. F. Wang, P. Davari, and F. Blaabjerg, "Robust fault ridethrough of converter-based generation during severe faults with phase jumps," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 570–583, Jan. /Feb. 2020.
- [17] Y. Z. Chang, J. B. Hu, W. Q. Y. Tang, and G. B. Song, "Fault current analysis of Type-3 WTs considering sequential switching of internal control and protection circuits in multi time scales during LVRT," *IEEE Transactions on Power Systems*, vol. 33, no. 6, pp. 6894–6903, Nov. 2018.
- [18] D. Dong, B. Wen, P. Mattavelli, D. Boroyevich, and Y. S. Xue, "Gridsynchronization modeling and its stability analysis for multi-paralleled three-phase inverter systems," in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, 2013, pp. 439–446.
- [19] H. Wu and X. F. Wang, "Transient stability impact of the phase-locked loop on grid-connected voltage source converters," in 2018 International Power Electronics Conference, Niigata, 2018, pp. 2673–2680.
- [20] X. F. Wang, L. Harnefors, and F. Blaabjerg, "Unified impedance model of grid-connected voltage-source converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1775–1787, Feb. 2018.
- [21] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. S. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310– 321, Jan. 2015.
- [22] H. Wu and X. F. Wang, "Design-oriented transient stability analysis of grid-connected converters with power synchronization control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6473–6482, Aug. 2019.
- [23] H. Wu and X. F. Wang, "Transient angle stability analysis of gridconnected converters with the first-order active power loop," in 2018 IEEE Applied Power Electronics Conference and Exposition, San Antonio, TX, 2018, pp. 3011–3016.
- [24] L. B. Huang, H. H. Xin, Z. Wang, L. Q. Zhang, K. Y. Wu, and J. B. Hu, "Transient stability analysis and control design of droopcontrolled voltage source converters considering current limitation," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 578–591, Jan. 2019.
- [25] L. Harnefors, L. Zhang, and M. Bongiorno, "Frequency-domain passivity-based current controller design," *IET Power Electronics*, vol. 1, no. 4, pp. 455–465, Dec. 2008.



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