Mode-varying Cell Equalizer Based on Interleaved Parallel Multiple Transformers

Qixing Wu, Mingyu Gao, *Senior Member*, *IEEE*, and Huipin Lin

***Abstract*—In the application of long series batteries, there is always the phenomenon that multiple cells in a pack are unbalanced simultaneously. In view of this situation, a mode-varying cell equalizer topology based on interleaved parallel multiple transformers is proposed in this paper. Every unit in this equalizer can freely switch between LLC resonance mode and 3-state LC quasi-resonance mode. The boosting effect of LLC structure is used to reduce the number of transformer's total turns. When multiple equalizer units need to work in LLC mode simultaneously, interleaved parallel technology is used to limit secondary side equalization current ripple for long-term protection of battery life. A prototype was designed and built to validate the effect of a closed loop LLC mode control algorithm with a state-of-charge (SOC) based equalization scheme selection strategy. Experimental results including up to 88.52% efficiency in LLC mode with 90.7% efficiency in 3-state LC mode, and minute level balancing time show the proposed topology demonstrates excellent balancing performance.**

***Index Terms*—3-state LC quasi-resonance mode, interleaved parallel, LLC resonance mode, mode-varying, ZVZCS band.**

I. Introduction

With the release of low-carbon development plans by major countries in the world, the new energy industry is developing at high speed. Lithium-ion batteries are a relatively efficient, stable and green energy storage device. Electric vehicles, laptops, and smart grid energy storage devices all need long strings of Lithium-ion batteries [1]. However, a battery pack composed of a large number of Lithium-ion battery cells will always appear unbalanced, with the consistency and aging of the cells. The cells' state-of-charge (SOC) will gradually differ from other cells in the same string, and this difference will gradually expand over time. If not mitigated, it will reduce the capacity and life of these cells, and even directly damage these cells. Therefore, the battery cell equalizer is used as the solution to provide protection and extend battery run time.

A cell equalizer can be divided into passive solution and active solution. The passive solution [2], [3] has realized integrated circuit (IC) manufacturing, and its low cost is very suitable for large-scale production of new energy equipment [3]. However, this solution generates additional heat and cannot transfer power from one cell to another. The active solution includes adjacent cell to cell (ACTC) topology [4]–[6], direct cell to cell (DCTC) topology [7]–[11], cell to pack (CTP) or pack to cell (PTC) topology [12]–[20], their variant topology [21]–[28] and hybrid structure [29]–[31]. Traditional ACTC topology and DCTC topology generally use capacitor, inductor or their combination as an energy transfer element. Sometimes, a multi-winding transformer is also used in some DCTC topologies. ACTC topology can only equalize a pair of adjacent cells in the series battery pack, and multiple pairs of adjacent cells can be equalized at the same time. For example, Ye *et al*. [4] used 2-state LC resonators as ACTC topology. This topology can only achieve zero voltage gap (ZVG) equalization when the voltages of donor cell and acceptor cell meet a certain relationship with capacitor voltage. Shang *et al*. [5] improved [4] into a 3-state LC quasi resonator which could freely realize ZVG equalization by adding a discharge branch, and analyzed the mathematical relationship between its switching period and resonance parameters, as well as the influence of resonance parameters' different combinations on efficiency. The disadvantage of ACTC topology is that two non-adjacent cells can only be balanced indirectly. Actual equalization efficiency will also decline rapidly with the distance between them. In order to solve this problem, Mestrallet *et al*. [22] proposed a variant of an inductor based ACTC equalizer. This topology has some limitations, that is, the sum of donor and acceptor battery strings' lengths must be equal to the whole battery pack's length. Furthermore, if there are balanced cells in the donor or acceptor battery string, a useless equalization cannot be avoided.

DCTC topology can balance a pair of donor and acceptor at any position in the pack. Pham *et al*. [7] proposed a DCTC topology based on switch array and LLC resonator. The advantage of a LLC resonator is that a soft switching state can reduce energy loss. The LLC resonator in this topology works at the resonant frequency point and PWM control is used to adjust equalization speed. Its disadvantage is a large number of switches. Shang *et al*. [24] proposed two direct multi-cell to multi-cell topologies, one based on half bridge LC converter and the other based on matrix LC converter. Half

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bridge LC converter topology needs to use a large number of MOSFETs, whereas matrix LC converter topology can use relays as an alternative, so the relative cost is low. These two topologies both have fast equalization speed, and their highest energy efficiency can reach 87.9%. However, their volume will increase rapidly with the length of the battery pack. DCTC topology is often difficult to expand, and generally cannot balance multiple pairs of donor and acceptor at the same time, which means a limited equalization speed.

CTP or PTC topologies generally use a transformer as an energy transfer element, including the combined structure of switch array and DC/DC isolated converter [12], [18]–[20], multi-transformer structure [14], [15], [27], multi-winding transformer structure [16], [17], [28], etc. The CTP structure can quickly discharge an overcharged battery, whereas the PTC structure can quickly charge the undercharged battery. Qi *et al*. [18] proposed a topology composed of switch array and integrated cascade DC/DC converter. This topology has relatively small volume, can output continuous balanced current, small ripple and has little impact on battery life. However, the switch array needs to use a large number of switches, which is expensive and difficult to expand. Oriti *et al*. [27] proposed a topology based on multiple LLC converters. Its equalization energy, which comes from an external AC power supply, flows into each LLC converter through a rectifier and buck voltage regulator, and then the LLC converter outputs equalization current to each target cell. Each LLC converter uses a fixed switching frequency, which can make the primary side switch in Zero-voltage-switching-on (ZVS) state and the secondary side rectifier diode in Zero-current-switching-off (ZCS) state. The operating frequency band that can meet this state is called ZVZCS frequency band. This kind of multi-transformer topology has the advantages of simple control, easy modularization and strong extendibility. It can realize multi-channel simultaneous equalization to realize fast equalization, but volume is relatively large. In [28], Shang *et al*. proposed a topology that can realize PTC and DCTC equalization at the same time. This topology is based on a multi-winding transformer, which uses fewer switches, and improves efficiency to more than 92% through synchronous rectification technology. However, when voltage between the cells in the battery pack is very close, this topology can only perform PTC equalization, and DCTC equalization will automatically terminate, which means actual equalization speed will slow down. This kind of multi-winding transformer structure always has a large volume, and its extendibility is limited by the manufacturing difficulty and cost of the transformer.

A hybrid topology is mainly layered equalization structure, that is, the whole pack is divided into several battery modules with the same length. Each battery module uses one equalization topology, and another topology is used for equalization between battery modules. For example, Peng *et al*. [31] proposed a topology that uses an inductor based ACTC structure inside each module and a pack to module equalization structure based on LLC resonators. This layered topology has hourly equalization speed, more than 92% efficiency of an intra module equalizer and 93.8% efficiency of pack to module equalizer. It can be seen the layered hybrid topology has great extendibility through modularization, so it is very suitable for long string battery packs.

In general, it can be known that efficiency, speed, component count, cost, control complexity and topology extendibility are general indicators to evaluate the performance of battery equalizer. This paper proposes a multi-transformer based cell equalizer topology with variable mode capability of free switching between CTP and ACTC. The topology takes the equalization circuit of two cells as an equalizer unit. Multiple equalizer units can operate in these two modes, respectively, at the same time without interference, and has enhanced extendibility. When the unit of proposed equalizer works in CTP mode, the energy of the donor cell is transferred to the entire pack through the LLC converter. The interleaved parallel technology is used to limit the ripple of the secondary side equalization current as much as possible to protect battery life. When operation mode is switched to ACTC, the circuit operates as a 3-state LC quasi resonator, which can achieve high efficiency.

The main contributions of this paper are listed as follows:

1) A novel mode-varying cell equalizer topology with fast equalization speed, good efficiency, fewer transformer's total turns, smaller output current ripple and other comprehensive cost is proposed.

2) A comprehensive design method based on equalizer output current and power analysis is proposed to guide the hardware design of resonant tank.

3) A closed-loop LLC mode control algorithm is proposed, which can always keep ZVZCS state and output equalization power near maximum value.

4) A SOC based equalization scheme selection strategy is proposed; and verified by the prototype. It can realize fast equalization in static, charging and discharging states.

II. Proposed Equalizer

The proposed equalizer structure is shown in Fig. 1. The equalizer divides two adjacent cells into an equalizer unit. The number of the i-th equalizer unit is Gi, the primary side of the Gi unit is controlled by four switches GiQ1∼GiQ4, and its resonant cavity is composed of resonant capacitor GiCr, resonant inductor GiLr and transformer GiT; its secondary side is a bridge rectifier composed of four diodes, and a secondary side output switch GiQ5 controls the on-off state between the secondary side and the battery pack. When multiple equalizer units operate in LLC resonance mode at the same time, interleaved parallel technology is adopted to reduce the ripple of the secondary side output equalization current, that is, the interleaved parallel LLC resonance mode.

A. LLC Resonance Mode

The proposed equalizer uses a half-bridge boost LLC structure, and its operation method is shown in Fig. 2. LC resonant circuit can boost voltage in a certain frequency range. At the same time, it enters ZVZCS state, which means primary switches enter the ZVS state, and the secondary diodes enter the ZCS state, to effectively reduce switching loss and electromagnetic interference [31] of the equalizer.

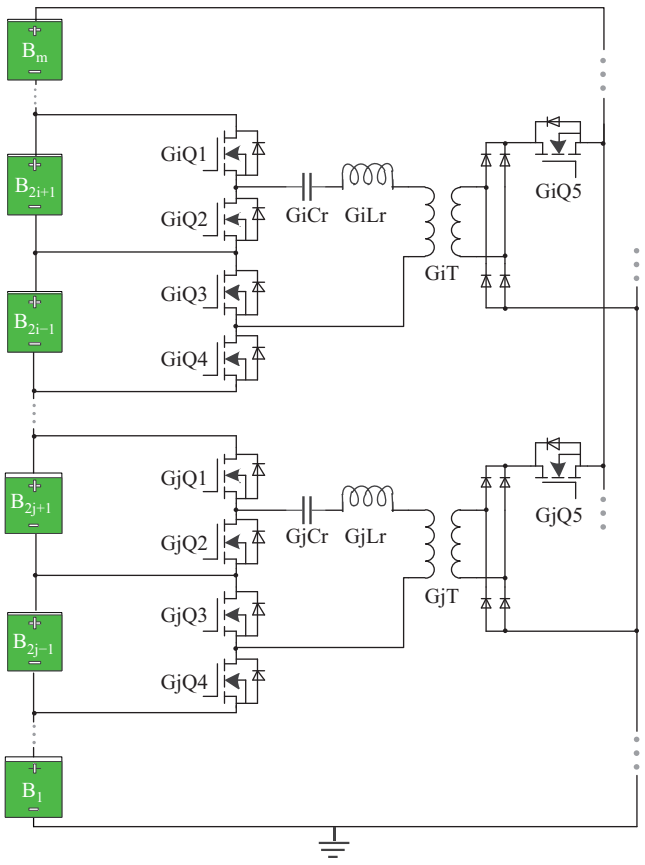


Fig. 1. The proposed equalizer structure.

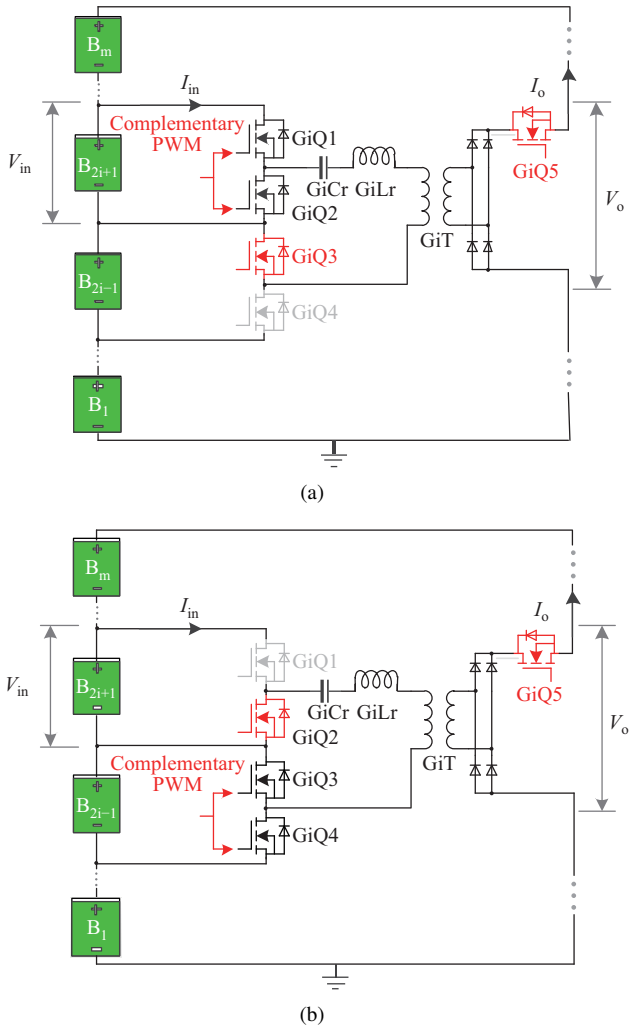


Fig. 2. The working process of LLC resonance mode. (a) When cell B_{2i+1} is used as a donor cell. (b) When cell B_{2i-1} is used as a donor cell.

Hereinafter, ZVZCS working frequency band is referred to as this operation band. Furthermore, it can replace part of the step-up transformer, thereby total turns and volume of the transformer are reduced.

In Fig. 2, V_{in} is the voltage input to the equalizer unit from the donor cell, V_{o} is the output voltage of equalizer unit, I_{in} is the input current of the primary side, and I_{o} is the output current of the secondary side. When the cell B_{2i+1} is used as the donor cell, the switches GiQ1 and GiQ2 are alternately turned on by a complementary switching signal with a duty cycle of 50%, GiQ3 is always on and GiQ4 is always off. When cell B_{2i-1} is used as the donor cell, switches GiQ3 and GiQ4 are alternately turned on, GiQ2 is always on and GiQ1 is always off.

B. Interleaved Parallel LLC Resonance Mode

In a long string of battery packs, there may be multiple overcharged cells at the same time. When a CTP equalizer with multi-transformers is used, CTP equalization can be carried out on multiple cells meeting equalization conditions. However, when multiple transformers output equalization current to the battery pack in discontinuous current mode (DCM) at the same time, the ripple of equalization current is large, which has an adverse effect on battery life [18]. The proposed equalizer adopts an interleaved parallel method as a solution. The switching waveforms of the equalizer units working in this mode simultaneously are phase-shifted in order, and the peaks of these units' output current are staggered. Thereby the ripple of multiple channels' total current can be limited without adding any hardware. Moreover, due to the unidirectional conduction characteristic of the diode, the secondary side ZCS state of every unit will not be affected by each other. Assume the units working simultaneously in the LLC mode are from the unit Gi to the unit G(i+k). The phase-shifting phase angle of unit Gj, which is represented by $\theta(j)$, should be:

$$\theta(j) = (j-i)\frac{\pi}{k+1} \quad (i \le j \le i+k) \tag{1}$$

The unit whose switching waveform is not phase-shifted is called the master unit of interleaved parallel LLC mode, and the other LLC units needing phase-shifting are called the slave units. For example, in Fig. 3, equalizer units Gi and Gj are output together in the interleaved parallel LLC resonance mode. Unit Gi is the main unit, then unit Gj is used as the slave unit driven by the complementary switching signal with a 90° phase shift.

However, each unit in the interleaved parallel LLC resonance mode is required to work at the same switching frequency. When the operation frequency bands of master and slave units do not overlap or their overlapping interval is too small, the interleaved parallel mode is hard to be turned on.

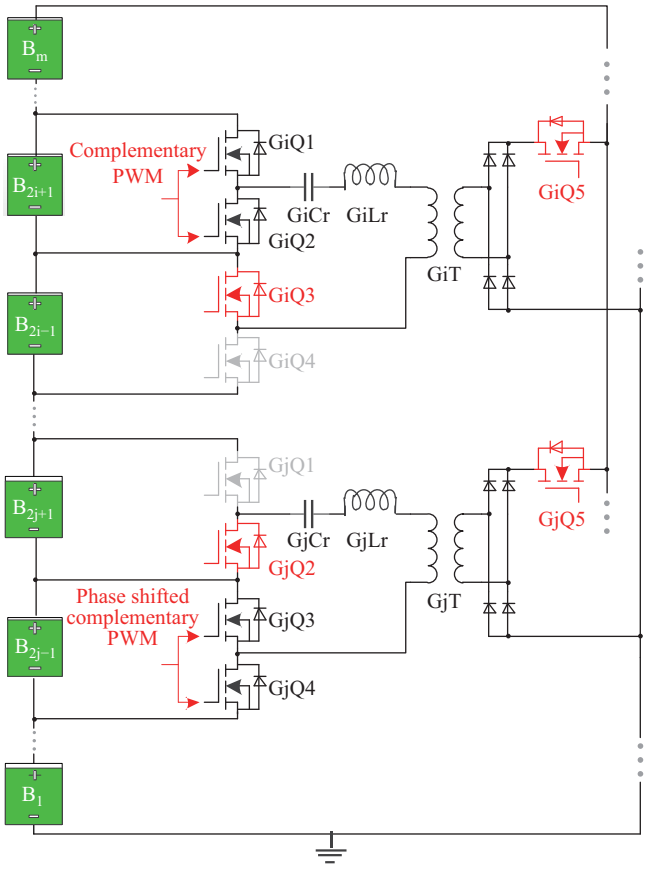


Fig. 3. The working process of interleaved parallel LLC resonance mode.

C. 3-state LC Quasi-resonance Mode

A 3-state LC quasi-resonance equalization circuit structure can realize zero voltage difference (ZVG) equalization. A 3-state LC quasi-resonator can release the capacitor's residual charge before the start of the next switching cycle by inserting an additional quasi-resonant state in the end of one switching cycle [5]. In the proposed equalizer, the same LLC resonant circuit is reused as the 3-state quasi-resonator. The transformer excitation inductance L_{m}, leakage inductance L_{f} and resonant inductor L_{r} are connected in series to form the quasi-resonant inductor, and the resonant capacitor C_{r} is used as the quasi-resonant capacitor.

III. The Design of Proposed Equalizer

$LiFePO_4$ cell is taken as the equalization object to design the proposed equalizer. The rated capacity of $LiFePO_4$ cell is 1.1 Ah, and the charge/discharge voltage is generally limited to 2.2 V to 3.6 V.

A. Analysis of DC Voltage Gain and Transformer Turns Ratio in LLC Resonance Mode

The equalizer performs CTP equalization in LLC resonance mode. The ratio of input voltage to output voltage of cell equalizer has a wide variation range. When each cell in the battery pack is in the charging and discharging platform, the voltage difference is also small between the two cells with relatively large SOC difference. In this state, voltage of the

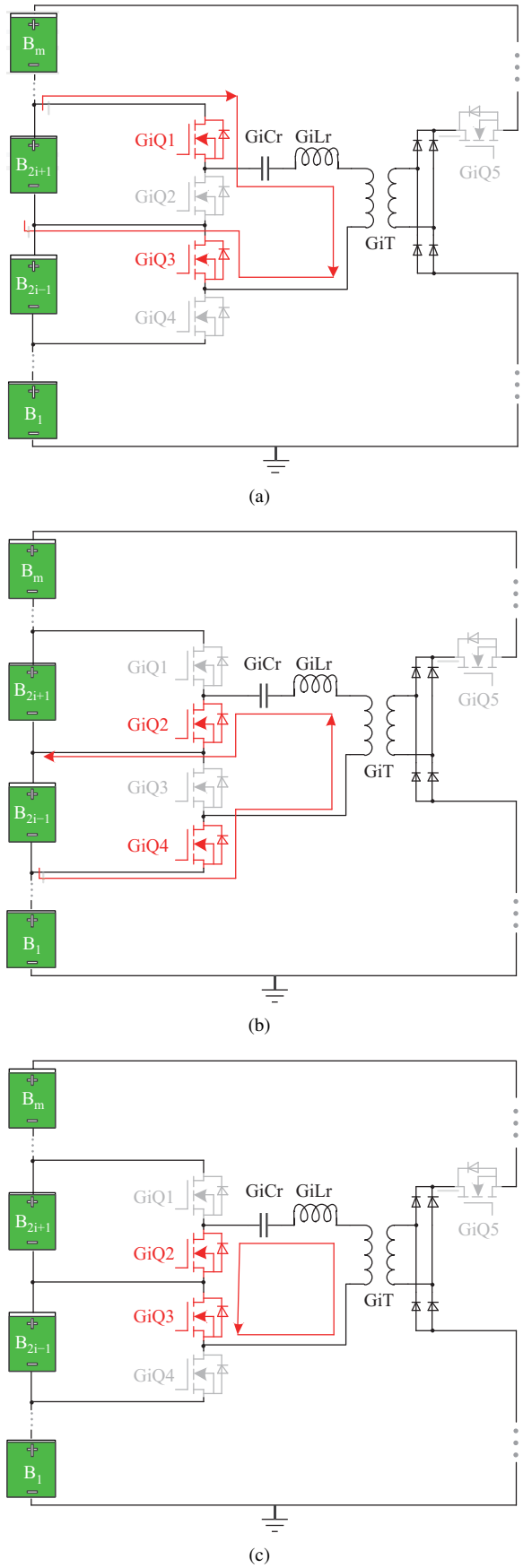


Fig. 4. The working process of 3-state LC quasi-resonant mode. (a) Quasi-resonant 1st state (Donor discharge). (b) Quasi-resonant 2nd state (Acceptor charging). (c) Quasi-resonant 3rd state.

selected donor cell is close to the average voltage of the battery pack. In addition, there is an extreme situation in the charging process: the initial voltage of the donor cell is close to the upper limit voltage of 3.6 V, and the other cells are all close to the lower limit voltage of 2.2 V. Therefore, for the equalizer with m series connected cells as the equalization object, the DC voltage gain $M_{\rm dc}$ design range of each equalizer unit is as follows:

$$M_{\rm dc}=\frac{V_{\rm o}}{V_{\rm in}}=\frac{1}{2n}M\in\left(\frac{2.2}{3.6}(m-1)+1,m\right] \tag{2}$$

where M is the normalized DC voltage gain, and m is the number of cells connected in series in the battery pack.

The design of the transformer turns ratio is related to the setting of the equalizer unit's operating point.

Method 1: The equalizer's operating point when all cells are in the charging and discharging platform is set near the LLC resonator's resonance point (where M is equal to 1). In order to avoid zero output state, the transformer turns ratio n should at least satisfy:

$$n_1=\frac{1}{2m} \tag{3}$$

Method 2: The equalizer's operating point in the extreme situation mentioned above is set near the resonance point, the operating point in the charging and discharging platform is set near the maximum point of the normalized DC voltage gain M. This is equivalent to using the boosting effect of the LLC resonator to replace part of the step-up transformer's role. Then the transformer turn ratio can be designed as:

$$n_2=\frac{1}{\frac{4.4}{3.6}(m-1)+2} \tag{4}$$

Meanwhile, in order to ensure that every equalizer unit will not enter the zero-output state when working in the charging and discharging platform, the maximum value $M_{\rm max}$ of the normalized DC voltage gain in Method 2 should at least meet the following conditions:

$$M_{\rm max}\geq\frac{m}{\frac{2.2}{3.6}(m-1)+1} \tag{5}$$

Assuming the turns on the primary side of the transformer is 1, the trends of the transformer's total turns N under the two design methods with increase in the series connected cells' number m are as follows:

It can be seen from Fig. 5 that as the number of series connected cells increases, the design according to the Method 2 above can significantly reduce the transformer's total turns, thereby its manufacturing cost and volume is reduced. Moreover, when the cells in the battery pack are seriously unbalanced, the operating point near the LLC resonance point can also ensure a quicker discharge of the donor cells.

B. Design of Resonant Tank Parameters

All the discussions below take the battery pack composed of 6 strings of $LiFePO_4$ cells as an example. According to the requirements of (4) and (5), the transformer turns ratio is $n=1/8$, and the maximum value of the normalized DC voltage gain must meet at least $M_{\rm max}\geq 1.5$.

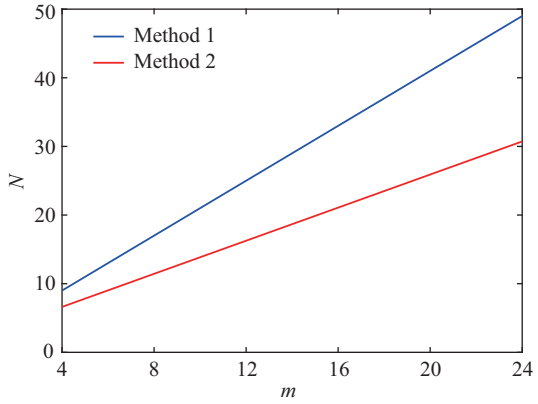


Fig. 5. The trends of the transformer's total turns N with the number m of series connected cells.

Now, the values of resonant inductance, resonant capacitance and transformer excitation inductance need to be designed. It is worth noting that resonant capacitance and resonant inductance affect the proposed equalizer unit's operating characteristics of LLC mode and 3-state LC mode at the same time.

In interleaved parallel LLC mode, since every equalizer unit involved operates in secondary side discontinuous current mode (DCM), the multiple units' total secondary side output current ripple is affected by the pulse width of each unit's secondary side output current. If the pulse width of each unit's secondary side current becomes wider, the overlapping part of the current pulse also becomes wider, and the ripple of the total secondary side current becomes smaller. Moreover, the pulse width of each equalizer unit's secondary output current is affected by different resonant inductance and capacitance combinations.

Figure 6 shows the waveforms of primary side resonance current $I_{\rm p}$, transformer excitation current $I_{\rm Lm}$ and secondary side output current $I_{\rm o}$ in LLC mode. $T_{\rm d}$ is the discharge time width of the primary side switch's output capacitance, $T_{\rm p}$ is the intersection time width of the primary side current and the excitation current, $T_{\rm bal}$ is the time width of the secondary side output current, and $T_{\rm s}$ is the switching cycle. They have the following relationship:

$$T_{\rm bal}=T_{\rm p}+T_{\rm d} \tag{6}$$

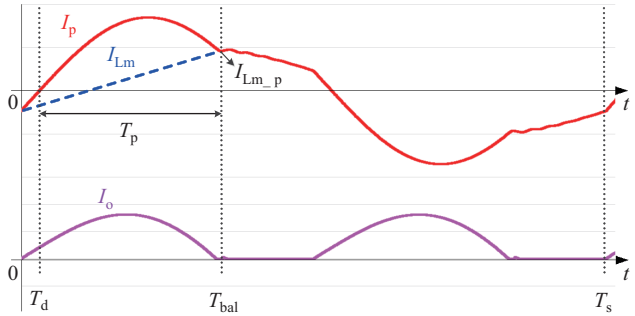


Fig. 6. Waveforms of primary side resonant current, transformer excitation current and secondary side output current in LLC mode.

In addition, the primary input current I_{p} and excitation current I_{Lm} during secondary side output current to battery pack can be expressed as follows:

$$\begin{cases} I_{\mathrm{p}} = I_{\mathrm{p\_p}} \sin\left[2\pi f_{\mathrm{r}}(t - T_{\mathrm{d}})\right] \\ I_{\mathrm{Lm}} = -\kappa I_{Lm\_\mathrm{p}} + \frac{nV_{\mathrm{o}}}{L_{\mathrm{m}}}(t - T_{\mathrm{d}}) \end{cases} \quad (T_{\mathrm{d}} \le t \le T_{\mathrm{bal}}) \tag{7}$$

where $I_{\mathrm{p\_p}}$ is the peak value of primary current, f_{r} is the resonant point frequency of LLC, κ is the ratio of initial value to peak value of transformer excitation current, I_{Lm_p} is the peak value of excitation current, L_{m} is the transformer excitation inductance. f_{r} and I_{Lm_p} can be obtained by the following equation:

$$\begin{cases} f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}} \\ I_{Lm\_\mathrm{p}} = \frac{nV_{\mathrm{o}}T_{\mathrm{p}}}{(1+\kappa)L_{\mathrm{m}}} \end{cases} \tag{8}$$

where L_{r} is the resonant inductance, C_{r} is the resonant capacitance, and V_{o} is the average value of the output voltage.

At T_{bal}, the primary side current and excitation current are equal, as follows:

$$I_{\mathrm{p\_p}} \sin(2\pi f_{\mathrm{r}} T_{\mathrm{p}}) = \frac{nV_{\mathrm{o}}T_{\mathrm{p}}}{(1+\kappa)L_{\mathrm{m}}} \tag{9}$$

Now, the above transcendental equation is approximately solved by expanding the sinusoidal part on the left as third-order power series, and the solution of the above equation is:

$$\begin{cases} T_{\mathrm{p}} = \frac{1}{2\pi f_{\mathrm{r}}}\sqrt{10 - 60\sqrt{\lambda/30 - 1/180}} \\ \lambda = \frac{nV_{\mathrm{o}}}{2\pi(1+\kappa)f_{\mathrm{r}}L_{\mathrm{m}}I_{\mathrm{p\_p}}} \end{cases} \tag{10}$$

where λ is the influence factor of circuit parameters.

Assume that κ is 0.5, V_{o} is 20 V, $I_{\mathrm{p\_p}}$ is 1.5 A and T_{d} is 0.4 μs. The relationship between f_{r} and time width T_{bal} of the secondary side current pulse can be obtained as follows:

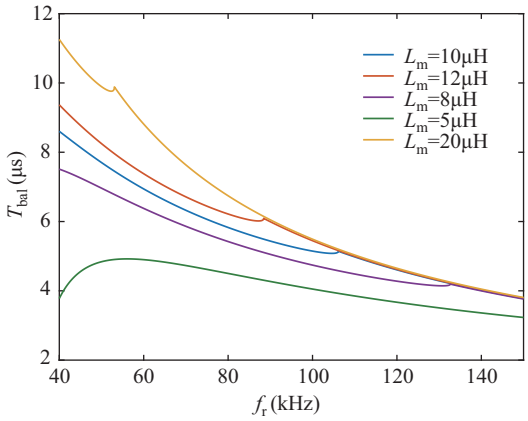


Fig. 7. Relationship between resonant frequency and time width of secondary output current pulse.

It can be seen that when $f_{\mathrm{r}} \ge 60$ kHz, if f_{r} becomes larger, the pulse width of secondary output current will become smaller in most cases. In order to verify the relationship between the ripple of the total secondary output current and the proposed equalizer's resonant frequency in interleaved parallel LLC mode, two different resonant frequencies for comparison need to be designed. Constrained by the dead time and the transient parameters of the switching device, the resonant frequency f_{r} value is designed to be within 150 kHz. So, the first value of f_{r} is designed as about 100 kHz and the second is designed as about 65 kHz.

On the other hand, in the 3-state LC mode, according to [5], if the ratio of resonant inductance to resonant capacitance is different, quasi-resonant current and energy efficiency will be affected. When this ratio becomes larger, quasi-resonant current becomes smaller and efficiency becomes higher; on the contrary, if the current is larger and efficiency is lower. For comparison, the first value of $L_{\mathrm{r}}/C_{\mathrm{r}}$ is designed as about 1 and the second is designed as about 8.

Thus, two sets of resonance parameters combinations need to be designed, as shown in Table I.

TABLE I
TWO PARAMETER COMBINATIONS OF RESONANT CAPACITOR AND RESONANT INDUCTOR

Parameter	Value	
	Comb. 1	Comb. 2
L_{r}	1.4 μH	6.8 μH
C_{r}	1.5 μF	0.87 μF

To ensure the comparative significance, the equalization test between these two sets of parameters need the same transformers, switches and diodes, and should be carried out under the same initial state of battery pack.

Next, an output power oriented fundamental analysis method is used to analyze and design the transformer excitation inductance.

The design value of transformer excitation inductance L_{m} has a direct impact on the range of the output power P_{o} and normalized DC voltage gain M of the equalizer in LLC modes.

The relevant equations of the normalized DC voltage gain M in LLC mode are as follows:

$$\begin{cases} M = M(\sigma) = \frac{1}{\sqrt{[1+r(1-\sigma^{-2})]^2 + Q^2(\sigma - \sigma^{-1})^2}} \\ r = (L_{\mathrm{r}} + L_{\mathrm{f}})/L_{\mathrm{m}} \\ \sigma = f_{\mathrm{s}}/f_{\mathrm{r}} \\ Q = \frac{\pi^2 I_{\mathrm{o}}\sqrt{L_{\mathrm{r}}/C_{\mathrm{r}}}}{8n^2 V_{\mathrm{o}}} = \frac{\pi^2 Y_{\mathrm{o\_eq}}}{8n^2}\sqrt{L_{\mathrm{r}}/C_{\mathrm{r}}} \end{cases} \tag{11}$$

where r is the inductance coefficient, L_{f} are the transformer leakage inductance, σ is the normalized frequency, Q is the quality factor, and $Y_{\mathrm{o\_eq}}$ is the secondary side equivalent load admittance, I_{o} is the average value of output current. Transformer leakage inductance L_{f} is temporarily ignored.

The output average power P_{o} is approximately calculated as:

$$P_{\mathrm{o}} = V_{\mathrm{o}} I_{\mathrm{o}} \tag{12}$$

By deforming (11), the theoretical calculation equation of the average output current I_{o} can be obtained as follows:

$$I_{\mathrm{o}} = \frac{8n^2 V_{\mathrm{o}}}{\pi^2}\sqrt{\frac{C_{\mathrm{r}}\left\{M^{-2} - \left[1 + r\left(1 - \sigma^{-2}\right)\right]^2\right\}}{L_{\mathrm{r}}\left(\sigma - \sigma^{-1}\right)^2}} \tag{13}$$

According to (12), (13) and the two resonance parameters combination in Table I, the curves of the average power P_{o} vs. the normalized frequency under different L_{m} values are obtained separately, as shown in Fig. 8.

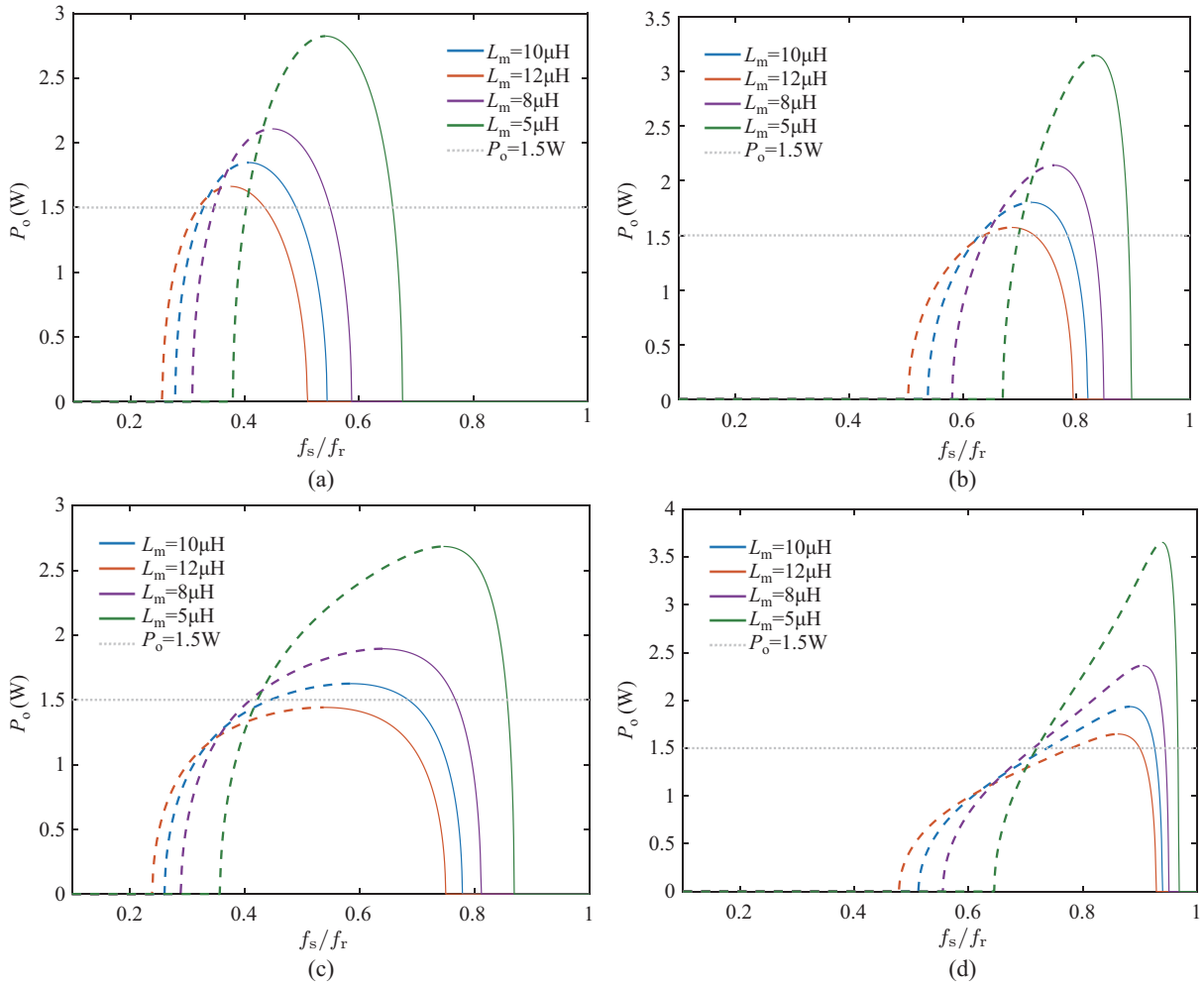


Fig. 8. The average power P_o vs. the normalized frequency under different L_m values. (a) Comb. 1 situation when $V_o = 21.6$ V, $M = 1.5$. (b) Comb. 2 situation when $V_o = 21.6$ V, $M = 1.5$. (c) Comb. 1 situation when $V_o = 15.8$ V, $M = 1.1$. (d) Comb. 2 situation when $V_o = 15.8$ V, $M = 1.1$.

In Fig. 8, the solid line part of the curve indicates the equalizer works in the ZVZCS frequency band, and there is a zero output critical frequency f_0 in the ZVZCS band. When the switching frequency is greater than or equal to f_0, the equalizer unit output power will be reduced to 0. According to Fig. 8(a) and (b), the equalizer unit's ZVZCS operating frequency band moves towards high frequency as L_m value decreases. This causes increasing switching loss. In addition, the ZVZCS band becomes narrower at the same time. Narrow bandwidth means rising difficulty of ensuring that each unit's ZVZCS band can overlap, because of the influence of actual hardware parameters in consistency. Thus, the interleaved parallel LLC resonance mode will be more difficult to be turned on. As a compromise between the equalizing speed and the difficulty to turn on interleaved parallel LLC mode for battery life protection, maximum output power is designed to be around 1.5 W.

Figure 8(c) and (d) theoretically estimate performance of equalizer units when the extreme imbalance situation mentioned above is approached. Maximum output power for both Comb. 1 and Comb. 2 increase slightly compared with Fig. 8(a) and (b), but output voltage has been greatly reduced from 21.6 V to 15.8 V. This indicates the actual secondary output current both Comb. 1 and Comb. 2 have increased significantly.

Comparing Fig. 8(a) with Fig. 8(c) and Fig. 8(b) with Fig. 8(d) respectively, it can be seen that when each cell in the battery pack is in the battery charging and discharging platform, the switching frequency f_s of LLC mode needs to be close to f_m (the frequency of normalized DC voltage gain's maximum point). This can obtain the fastest equalization speed and avoid the secondary side sliding into the zero-output state. At this time, the secondary side outputs equalization current in DCM. When the voltage value of the donor cell and the battery pack make the normalized DC voltage gain close to the lower limit in (2), f_s moves closer to the resonant frequency f_r, and the secondary side outputs equalization current in a nearly continuous current mode (CCM).

According to (11) and the two resonance parameter combinations in Table I, when battery pack voltage V_o is 21.6 V and average output power P_o of LLC mode is 1.5 W, the curves of normalized voltage gain vs. normalized frequency at different L_m values are drawn respectively, as shown in Fig. 9.

According to Fig. 9, in LLC mode, if L_m value is large, the maximum value M_{max} of normalized DC voltage gain is small. In order to meet $M_{max} \geq 1.5$, L_m value should not be

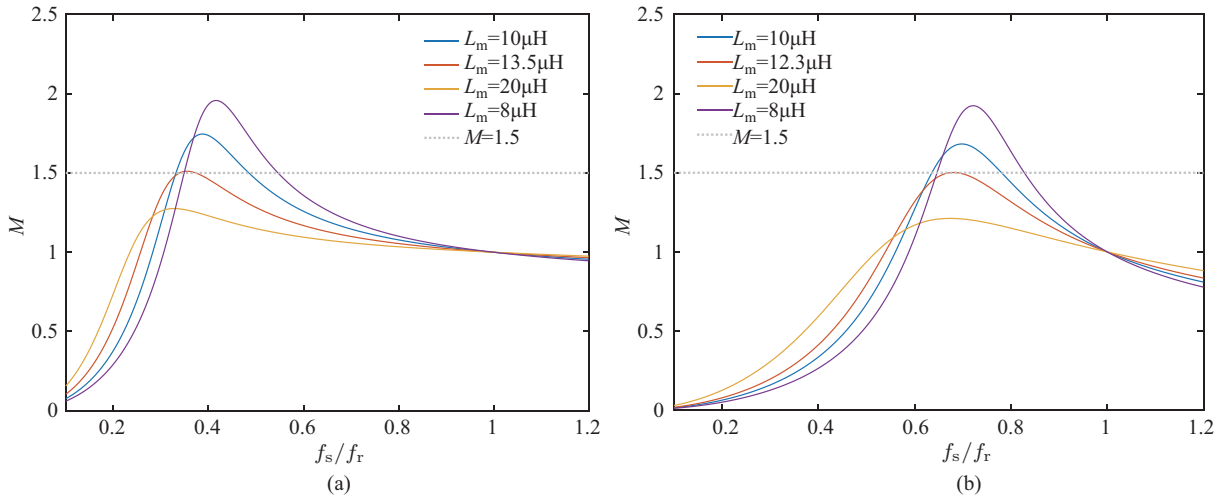


Fig. 9. The normalized voltage gain vs. normalized frequency at different L_{m} values when $V_{\mathrm{o}} = 21.6$ V, $P_{\mathrm{o}} = 1.5$ W. (a) Comb. 1 situation. (b) Comb. 2 situation.

designed too large. In Fig. 9(a), when the L_{m} value is 13.5 μH, and in Fig. 9(b), when the L_{m} value is 12.3 μH, $M_{\max}$ is very close to 1.5. The upper limit of L_{m} value needs to be 12 μH, by comparing the curves under Comb. 1 and Comb. 2.

Furthermore, for 3-state LC quasi-resonance mode, if the ratio of total resonance inductance to capacitance becomes larger, equalization current becomes smaller, and efficiency becomes higher [5]. Therefore, in the proposed structure, the L_{m} value should not be too small to ensure a suitable equalization speed and efficiency.

In conclusion, L_{m} value should be designed between 10 μH and 12 μH.

IV. Power Loss Analysis

A. LLC Resonance Mode

In LLC mode, the total power loss p_{loss} of the proposed equalizer consists of three main components:

$$p_{\mathrm{loss}} = p_{\mathrm{pri}} + p_{\mathrm{sec}} + p_{\mathrm{trans}} \tag{14}$$

where p_{pri} is the primary circuit loss, p_{sec} is the secondary circuit loss, and p_{trans} is the transformer loss.

The components of primary circuit loss are as follows:

$$\begin{cases} p_{\mathrm{pri}} = p_{\mathrm{pri\_con}} + p_{\mathrm{pri\_sw\_onoff}} \\ p_{\mathrm{pri\_con}} = p_{\mathrm{pri\_sw\_con}} + p_{\mathrm{LrCr\_con}} \end{cases} \tag{15}$$

where $p_{\mathrm{pri\_con}}$ is the conduction loss of the primary circuit, $p_{\mathrm{pri\_sw\_onoff}}$ is the switching loss of the primary circuit, $p_{\mathrm{pri\_sw\_con}}$ is the conduction loss of the primary semiconductor switches, $p_{\mathrm{LrCr\_con}}$ is the conduction loss caused by parasitic resistance of the primary resonant elements and PCB line.

Therefore, the conduction loss of the primary circuit can be further expressed as:

$$p_{\mathrm{pri\_con}} = I_{\mathrm{pri\_rms}}^2 R_{\mathrm{pri\_con}} \tag{16}$$

where $I_{\mathrm{pri\_rms}}$ is the effective value of primary side current, $R_{\mathrm{pri\_con}}$ is the total conduction resistance of the primary circuit without the primary coil of the transformer.

For the switching loss of the primary circuit, since the LLC mode can achieve ZVS turn-on state, it only includes the turn-off loss $p_{\mathrm{pri\_sw\_off}}$. This loss can be expressed as [32]:

$$\begin{cases} p_{\mathrm{pri\_sw\_onoff}} = p_{\mathrm{pri\_sw\_off}} \\ p_{\mathrm{pri\_sw\_off}} = \frac{V_{\mathrm{in}}}{3}\left(\frac{V_{\mathrm{o}} t_{\mathrm{off}}}{4nL_{\mathrm{m}}} - C_{\mathrm{pri\_oss}} V_{\mathrm{in}} f_{\mathrm{sw}}\right) \end{cases} \tag{17}$$

where $C_{\mathrm{pri\_oss}}$ is the output capacitance and t_{off} is the turn-off time of the primary side MOSFET. Due to $C_{\mathrm{pri\_oss}}$ is pf level, while the switching frequency of the proposed equalizer is kHz level, so $p_{\mathrm{pri\_sw\_off}}$ can be approximately as:

$$p_{\mathrm{pri\_sw\_off}} \approx \frac{V_{\mathrm{in}} V_{\mathrm{o}} t_{\mathrm{off}}}{12nL_{\mathrm{m}}} \tag{18}$$

This means that in ZVS turn-on state, the theoretical value of primary side switching loss is almost independent of the switching frequency but related to the input and output voltage of the equalizer.

Secondary circuit loss comes from conduction resistance of the secondary circuit, the forward on voltage of the rectifier diodes, and the turn-on loss of these diodes (secondary side ZCS turn-off state).

The loss of transformer mainly comes from planar magnetic core and PCB coil. This loss is affected by primary and secondary current, switching frequency and magnetic core temperature etc., together.

B. 3-state LC Quasi-resonance Mode

Energy efficiency of the 3-state quasi resonance mode can be expressed as follows [5]:

$$\begin{cases} \eta = \frac{V_{\mathrm{acceptor}}}{V_{\mathrm{donor}}} \frac{V_{\mathrm{donor}} - (1-\alpha)V_{\mathrm{acceptor}}}{(1-\alpha)V_{\mathrm{donor}} + \alpha V_{\mathrm{acceptor}}} \\ \alpha = \frac{\mathrm{e}^{-\pi\rho/\sqrt{1-\rho^2}}}{\sqrt{1-\rho^2}} \\ \rho = 0.5 R_{\mathrm{eq}} / \sqrt{(L_{\mathrm{m}} + L_{\mathrm{f}} + L_{\mathrm{r}})/C_{\mathrm{r}}} \end{cases} \tag{19}$$

where V_{donor} is the donor cell voltage and V_{acceptor} is the acceptor cell voltage, α is the impact factor of energy efficiency, ρ is the quasi-resonant coefficient, R_{eq} is the equivalent resistance including conduction loss and switching loss.

It is assumed that total primary side inductance of the transformer is 12 μH, and voltage of donor cell is the same as that of acceptor cell. MATLAB is used to draw the relationship between equivalent resistance and energy efficiency of 3-state LC quasi-resonance mode under both resonant parameters' combinations.

As can be seen from Fig. 10, when the equivalent resistance $R_{\rm eq}$ is the same, the efficiency of Comb. 2 is higher than of Comb. 1. With increase of $R_{\rm eq}$, efficiency will decline gradually.

V. The Control Strategy of The Equalizer Unit

A. Closed Loop Control Algorithm for LLC Mode Equalizer

According to (12) and Fig. 8, secondary output current $I_{\rm o}$ of LLC mode decreases monotonically in ZVZCS frequency band, and there is a maximum value $I_{\rm o\_max}$. Therefore, the equalizer unit can perform closed-loop PI control by using secondary output current $I_{\rm o}$ as the input and switching frequency $f_{\rm s}$ as the output. In order to speed up equalization speed, output current $I_{\rm o}$ needs to work near the value of $I_{\rm o\_max}$, which is used as the output current control command value $I_{\rm o}^*$. According to (13), if the resonance parameter is determined, the value of $I_{\rm o\_max}$ is related to battery pack voltage $V_{\rm o}$ and normalized DC voltage gain M.

Now, suppose $L_{\rm m}$ is 12 μH. Maximum current $I_{\rm o\_max}$ is calculated based on the frequency sweep method, and the curve of $I_{\rm o\_max}$ vs. $V_{\rm o}$ under different M values is obtained as Fig. 11.

In Fig. 11, because of the cell voltage range 2.2 V∼3.6 V, the output voltage $V_{\rm o}$ under different M values is limited to different ranges. It can be seen from Fig. 11 that under the same value of M, $I_{\rm o\_max}$ and $V_{\rm o}$ can be approximately regarded as a linear relationship, as follows:

$$I_{\rm o\_max} \approx Y_{\rm o\_eq}(M)V_{\rm o} \tag{20}$$

where $Y_{\rm o\_eq}(M)$ is the equivalent output admittance related to normalized DC voltage gain M value. In addition, under the same output voltage $V_{\rm o}$, the $I_{\rm o\_max}$ value increases as M value decreases. Therefore, for example, calculation results obtained by substituting $Y_{\rm o\_eq}(1.5)$ into (20) can be used as the current command value $I_{\rm o}^*$ within the range of $1.4 < M \leq 1.5$. In this way, current command value can be obtained by establishing a ladder-type data table of equivalent output admittance $Y_{\rm o\_eq}(M)$, thereby the calculation is simplified and MCU operation is speeded up. It is worth noting that in actual equalizer control, due to the existence of conduction loss and core loss, $Y_{\rm o\_eq}(M)$ needs to enlarge a certain margin according to the theoretical value in Fig. 11.

Then, in order to keep the LLC mode equalizer in the ZVZCS and non-zero output frequency band, the switching frequency control value from PI controller needs to be limited between the maximum M point frequency $f_{\rm m}$ and the zero-output critical frequency f_0. The maximum M point frequency $f_{\rm m}$ value can be obtained by the following method: according to (11), normalized DC voltage gain M is derived from the square of the normalized frequency σ^2, maximum M point frequency $f_{\rm m}$ can be obtained based on Cardin's root formula, as below:

$$f_{\rm m} = f_{\rm r}\sqrt{\sqrt[3]{\lambda+\sqrt{\lambda^2+\varepsilon}}+\sqrt[3]{\lambda-\sqrt{\lambda^2+\varepsilon}}}$$
$$\lambda = r^2/Q^2$$

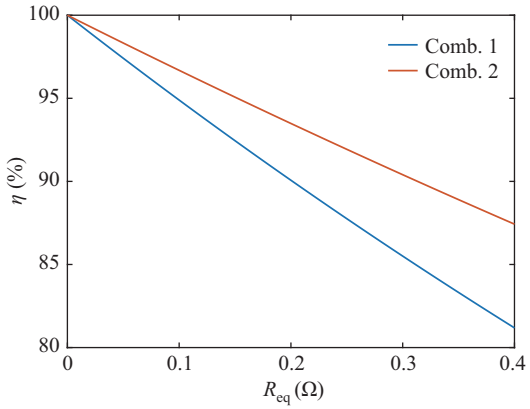


Fig. 10. Relationship between equivalent resistance $R_{\rm eq}$ and energy efficiency η of 3-state LC quasi-resonance mode.

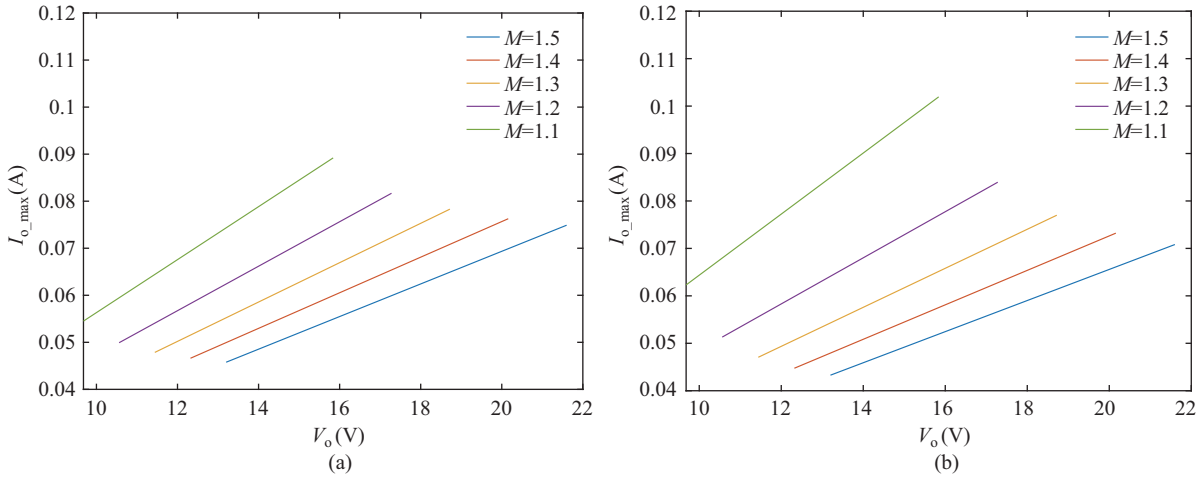


Fig. 11. $I_{\rm o\_max}$ vs. $V_{\rm o}$ under different M values. (a) Comb. 1 situation. (b) Comb. 2 situation.

$$\varepsilon = \left(\frac{2r^2+2r}{3Q^2} - \frac{1}{3}\right)^3 \tag{21}$$

According to (21), the maximum M point frequency f_{m} is related to the inductance coefficient r and the quality factor Q. The aforementioned two resonance parameters combination and the transformer magnetizing inductance L_{m} have determined the inductance coefficient r. According to (11) and (20), the equalizer's quality factor Q is changing and related to the equivalent output admittance $Y_{\mathrm{o\_eq}}(M)$. It means the quality factor Q is related to the normalized DC voltage gain M, which is determined by the current input and output voltage of the equalizer.

Therefore, when the equalizer unit is designed to work at the maximum point of M, its quality factor Q, and then the f_{m} value determined by Q are both related to the maximum M value $M_{\max}$. This relationship can be solved by MATLAB, as follows:

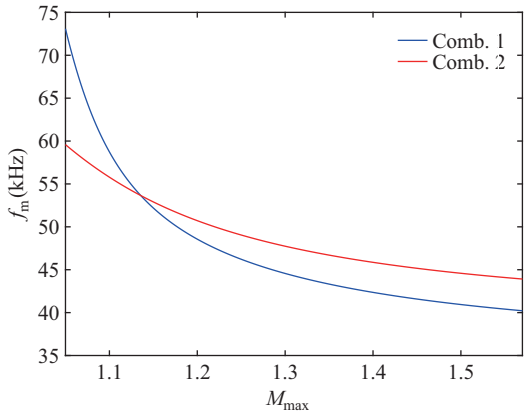


Fig. 12. f_{m} value vs. $M_{\max}$ value.

Similarly, the above data need to be discretized into a data table to write to MCU. Current $M_{\max}$ value is obtained by floating up one margin ΔM on the basis of feedback M value. Then this $M_{\max}$ value is used to query this data table to get the current f_{m} value as the lower limit of the switching frequency control value.

The zero-output critical frequency f_0 can be obtained by making (13) equal to 0, as follows:

$$f_0 = f_{\mathrm{r}}\sqrt{\frac{r}{r - M^{-1} + 1}} \tag{22}$$

The relationship between f_0 and the feedback M value is as follows:

Figure 13 is also discretized into a data table, and the controller queries the table according to the current feedback M value to determine the upper limit value of switching frequency. To sum up, the LLC mode closed-loop controller of the equalizer unit can be described as shown in Fig. 14.

Table A in Fig. 14 is the data table of the equivalent output admittance $Y_{\mathrm{o\_eq}}(M)$ about the feedback M value described above. Table B in Fig. 14 is the data table of the f_{m} value about the $M_{\max}$ value. Table C in Fig. 14 is the data table of f_0 value vs. the feedback M value.

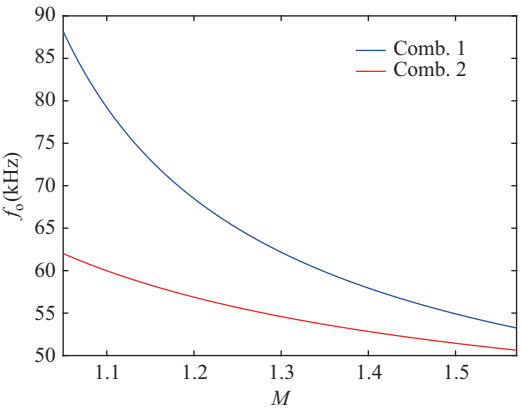


Fig. 13. The curve of zero output critical frequency f_0 vs. the M feedback value.

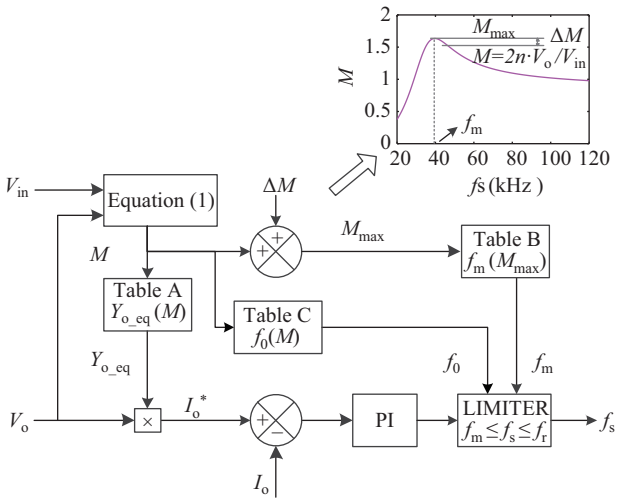


Fig. 14. LLC mode closed loop controller.

B. Interleaved Parallel LLC Resonance Mode and Its Necessary Condition

When the number of series cells in the battery pack is 6, the proposed equalizer is designed to keep at most, two units for CTP equalization at the same time.

A comparative simulation experiment is carried out with MATLAB 2018 Simulink to illustrate the limiting effect of interleaved parallel mode on output current ripple. The switching frequency is fixed to 50 kHz. Except for two sets of resonance parameters combination Comb. 1 and Comb. 2, other parameters are shown in Table II, and the waveform diagram is shown in Fig. 15.

TABLE II
OTHER PARAMETERS IN LLC MODE SIMULATION EXPERIMENT

Parameter	Value	Parameter	Value
$V_{\mathrm{donor\_G1}}$	3.32 V	L_{f}	0.2 μH
$V_{\mathrm{donor\_G2}}$	3.29 V	C_{oss}	282 pF
V_{o}	19.5 V	$R_{\mathrm{MOS\_on}}$	8.5 mΩ
n	1/8	C_j	35 pF
L_{m}	12 μH	V_{D}	0.42 V

Where $V_{\mathrm{donor\_G1}}$ is the initial voltage of donor cell in interleaved parallel LLC main unit G1, $V_{\mathrm{donor\_G2}}$ is the initial

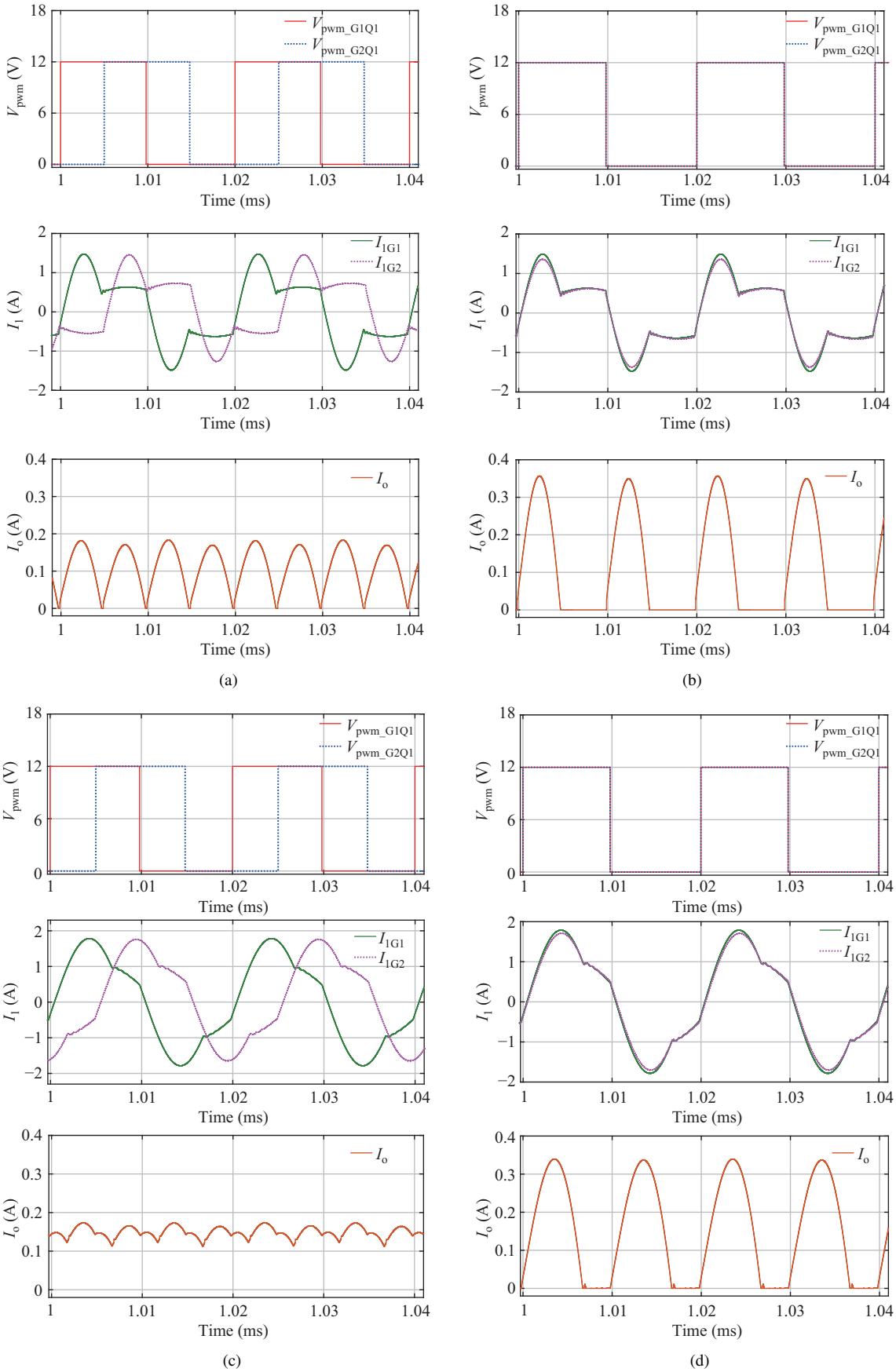


Fig. 15. Simulation waveform of interleaved parallel and non-interleaved parallel LLC resonant mode. (a) Interleaved parallel LLC mode with Comb. 1. (b) Non-interleaved parallel LLC mode with Comb. 1. (c) Interleaved parallel LLC mode with Comb. 2. (d) Non-interleaved parallel LLC mode with Comb. 2.

voltage of the donor cell from slave unit G2, $V_{\rm o}$ is the initial voltage output from the secondary side to the battery pack, n is the transformer turn ratio, $L_{\rm m}$ is the transformer excitation inductance, $L_{\rm f}$ is the transformer leakage inductance, $C_{\rm oss}$ is the output capacitance of the primary MOSFET, $R_{\rm MOS\_on}$ is the conduction resistance of the primary MOSFET, C_j is the junction capacitance of the secondary rectifier diode, and $V_{\rm D}$ is the forward voltage drop of the secondary diode.

In Fig. 15, $V_{\rm pwm\_G1Q1}$ and $V_{\rm pwm\_G2Q1}$ are the driving waveforms of switch G1Q1 and switch G2Q1, with a 90° phase difference between them when the interleaved parallel LLC mode turns on. $I_{1\rm G1}$ and $I_{1\rm G2}$ are the primary resonance currents of the equalizer units of the G1 and G2 units respectively, and $I_{\rm o}$ is the sum of the current output from the secondary side of the G1 unit and G2 unit. By comparing the figures in Fig. 15, it can be observed that in interleaved parallel LLC resonance mode, peak value of the current ripple is only half that in non-interleaved parallel LLC resonance mode. The secondary side output current pulse width of Comb. 1 is smaller than of Comb. 2, which is the same as the change trend in Fig. 8.

As mentioned above, all equalizer units in interleaved parallel LLC resonance mode need to share the same switching frequency. If any unit falls out of ZVZCS state at this switching frequency or enters zero output state, interleaved parallel LLC mode should not be turned on. Therefore, whether each unit enters the interleaved parallel LLC mode needs to meet the necessary condition first. According to the algorithm in Fig. 14, the control range of the switching frequency under different M values is obtained as shown in Fig. 16.

The shaded frequency band in Fig. 16 is the control range of the switching frequency under different M values. It is assumed the operating frequency bands of each unit completely overlap. Therefore, the necessary condition for interleaved parallel LLC mode is at a common switching frequency, each equalizer unit can work in the shaded frequency band in Fig. 16. According to the above necessary condition, the equalizer unit with higher voltage donor cell should be selected as the master unit, the equalizer unit with lower voltage donor cell is selected as the slave unit, and the common switching frequency is determined by the feedback data of the master unit. The slave unit's frequency follows the master unit. Therefore, the operating point of the slave unit always falls to the left side of the master unit.

As long as the distance between the two equalizers' operating points meets certain conditions, the slave unit is sure to work in the ZVZCS band. In Fig. 16(a), the shortest distance between the maximum point frequency curve and the zero-output critical frequency curve in the horizontal axis direction is observed to be nearly 0.14, whereas in Fig. 16(b) this distance is nearly 0.12, therefore, (23) is designed as the necessary condition to determine whether the interleaved parallel LLC mode is turned on.

$$\delta = \begin{cases} 0 & M_{\rm slave} - M_{\rm master} \le 0.1 \\ 1 & M_{\rm slave} - M_{\rm master} > 0.1 \end{cases} \tag{23}$$

where δ is the disabled flag of interleaved parallel LLC mode, $M_{\rm master}$ is the main unit's normalized DC voltage gain feedback value, and $M_{\rm slave}$ is the slave unit's normalized DC voltage gain feedback value. When $\delta = 0$, the interleaved parallel LLC mode is enabled, when $\delta = 1$, the mode is disabled.

C. Control Strategy of 3-state LC Quasi-resonance Mode

The 3-state LC quasi-resonant mode adopts fixed switching frequency control. According to [5], the estimation formula of switching frequency is as follows:

$$f_{\rm s} = \frac{\sqrt{1 - \frac{C_{\rm r} R_{\rm on}^2}{4(L_{\rm m}+L_{\rm f}+L_{\rm r})}}}{3\pi\sqrt{(L_{\rm m}+L_{\rm f}+L_{\rm r})C_{\rm r}}} \tag{24}$$

where $R_{\rm on}$ is the conduction resistance in the resonant cavity, $C_{\rm r}$ and $L_{\rm r}$ are the resonant capacitance and resonant inductance respectively, $L_{\rm m}$ and $L_{\rm f}$ are the transformer excitation inductance and leakage inductance, respectively.

VI. Overall System Framework and SOC based Equalization Scheme Selection Strategy

The overall framework of the proposed cell equalizer is as Fig. 17. The SOC based equalization scheme selection strategy is as Fig. 18.

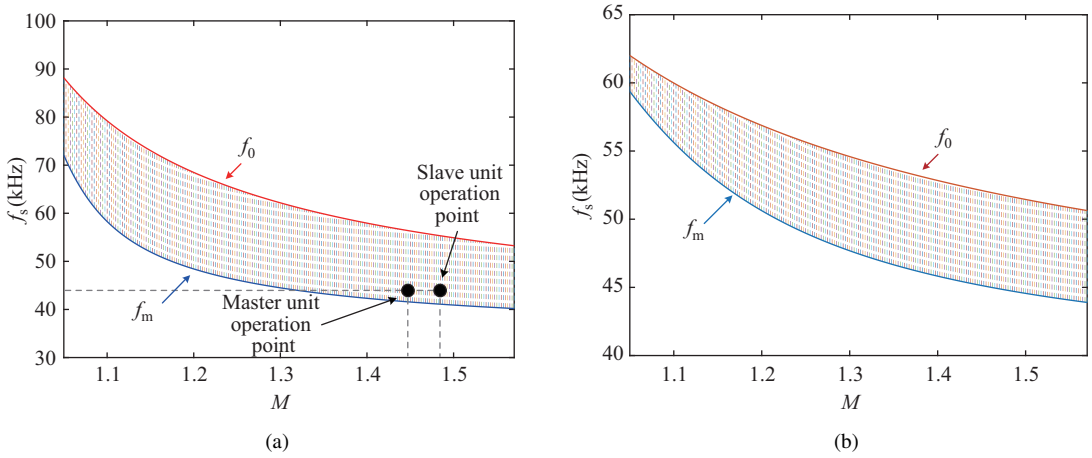


Fig. 16. Control range of switching frequency under different M values. (a) Comb. 1 situation. (b) Comb. 2 situation.

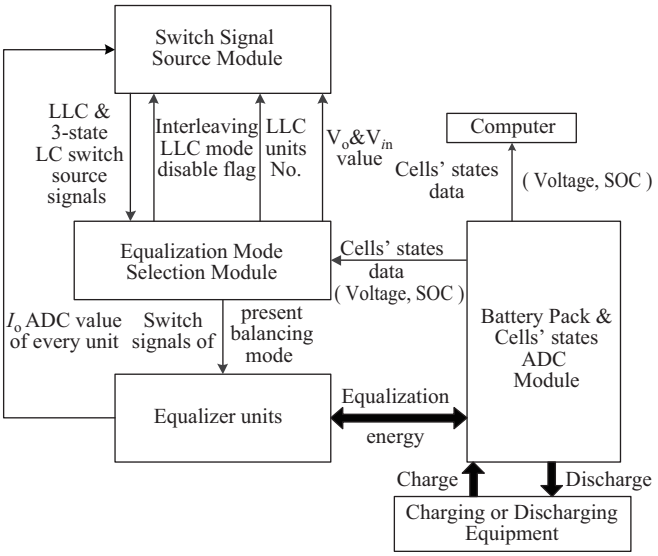


Fig. 17. The overall framework of the proposed cell equalizer.

The description of Fig. 17 is as follows:

a) Battery pack and cells state ADC module samples the voltage and current of each cell and calculates its SOC value. Then the information is sent to the equalization mode selection module and the computer, respectively.

b) The equalization mode selection module selects the equalization scheme according to the current, voltage and SOC data of each cell, and judges the value of the interleaved parallel LLC mode disable flag δ. Then, it sends the feedback value of δ, the equalizer unit number in LLC mode, and the average value of the input and output voltages ($V_{\rm in}, V_{\rm o}$) to the switch signal source module. After the response from the switch signal source module is obtained, the equalization mode selection module correctly distributes the switch source signal to 15 switch drive channels and sends them to all 3 equalizer units.

c) If δ is 0, the switching signal source module selects the secondary output current $I_{\rm o}$ sampling value of the main LLC unit according to the number, updates the LLC switching

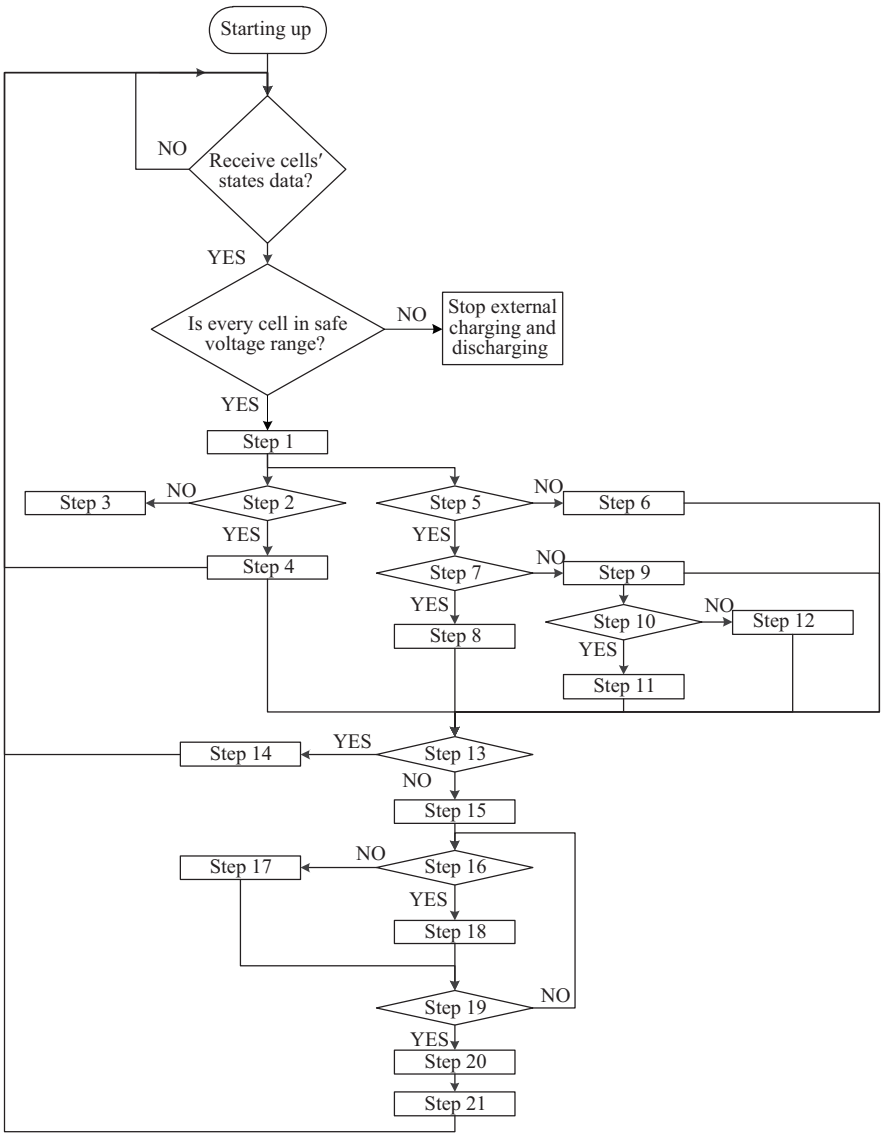


Fig. 18. SOC based equalization scheme selection strategy.

frequency according to the algorithm in Fig. 14, and shifts the phase of the slave LLC unit switching signal. If δ is 1, the switching signal source module updates the LLC switching frequency of each unit separately.

The operating strategy of the equalization mode selection module is shown in Fig. 18. The system first detects whether the voltage of each cell in the battery pack is within the safe voltage zone. If not, it immediately stops the charging and discharging process of the battery pack by the external device. If yes, the subsequent steps are explained as follows:

Step 1: Cells state data processing: Calculate the average SOC of the entire battery pack (*SOC_avg1*), and the average SOC of each unit. Record the unit number X with the highest average SOC and the cell number x with the higher SOC in unit X, the second highest unit number Y and the cell number y with the higher SOC in unit Y, the lowest unit number Z and the cell number z with the higher SOC in unit Z, and the cell number w with the lowest SOC in the entire pack; calculate the average SOC (*SOC_avg2*) of the other two units except unit X; record the voltage values of cell x and cell y, and calculate the interleaved parallel LLC mode disable flag δ.

Step 2: Judge: is the absolute difference between the SOC of cell z and the average SOC in unit Z greater than 0.1%?

Step 3: Ready to select equalizer unit Z to enter standby mode.

Step 4: Ready to select equalizer unit Z to turn on the 3-state LC mode.

Step 5: Judge: is the absolute difference between the SOC of cell x (or cell w) and *SOC_avg1* greater than 0.1%?

Step 6: Ready to select equalizer unit X to enter standby mode.

Step 7: Judge: is the absolute difference between the SOC of cell y (or cell w) and *SOC_avg2* greater than 0.1%?

Step 8: Ready to select cell x and cell y to turn on parallel LLC mode.

Step 9: Ready to select cell x to start single unit LLC mode.

Step 10: Judge: is the absolute difference between the SOC of cell y and the average SOC in unit Y greater than 0.1%?

Step 11: Ready to select unit Y to turn on 3-state LC quasi-resonance mode.

Step 12: Ready to select equalizer unit Y to enter standby mode.

Step 13: Judge: is the current equalization scheme the same as the previous one?

Step 14: Send the voltage feedback data of the corresponding unit to the switching signal source module according to the last equalization scheme.

Step 15: Record this equalization scheme and close all switch drive channels.

Step 16: Judge: is interleaved parallel LLC mode disable flag δ equal to 0?

Step 17: Send the unit number X and Y, the voltage feedback data of these two units, and the value of δ to the switching signal source module.

Step 18: Send the main unit number X, the voltage feedback data of this unit, and the value of δ to the switch signal source module.

Step 19: Judge: Does equalization mode selection module receive the response that the switching signal source module has completed the control parameter update?

Step 20: Update the connection relationship between the switch source signals and all switch drive channels.

Step 21: Reopen all switch drive channels and output switch signals to all equalizer units.

It should be noted the operating modes of all equalizer units constitute an overall equalization scheme of the equalizer. In other words, the operating modes of each equalizer unit are switched together. If the overall equalization pre-scheme at the next moment is different from the current one, the equalization mode selection module will first close all connection channels, make all equalizer units suspend equalization and enter the intermediate standby state. After the scheme update is complete, the connection channels will be reopened. Then all equalizer units will start to operate in new modes, respectively.

VII. Hardware System Building and Experiment

In order to verify the proposed equalizer system, an experimental prototype with 6 strings of 1.1 Ah $LiFePO_4$ cells is built. The prototype contains 3 equalizer units, each unit uses the same type of switch, diode, resonant inductor and resonant capacitor. Each unit's transformer uses the same type of magnetic core, and the same number of winding turns. Consistency between equalizer units, including battery internal resistance, and component parameters, is adjusted by a closed loop control algorithm in Fig. 14 and battery safety voltage timing detection. The operation scene of the prototype system and external charging and discharging equipment is shown in Fig. 19.

A. Hardware System Building

The switching signal source module uses STM32F103C8T6 to complete the closed loop control of LLC mode, phase shift control of switching signal, and generates the fixed frequency switching signal of 3-state LC mode. The equalization mode selection module uses another STM32F103C8T6 to cooperate with the multiplex switches PI3B3253QEX to distribute the switch drive channels based on different equalization

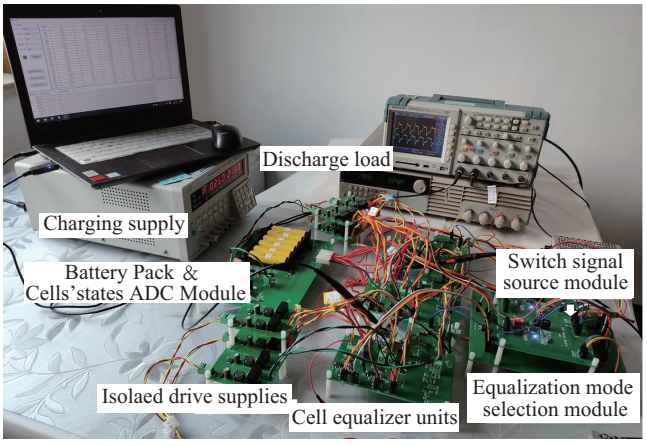


Fig. 19. The operation scene of the prototype system and external charging and discharging equipment.

schemes. The battery pack and cells state ADC module use STM32F405RGT6 to complete the current and voltage ADC and communication control.

In the design scheme of the equalizer units' main circuit, MOSFET BUK7K8R7-40EX with a small output capacitance and conduction resistance is selected as the primary side switch. In order to further reduce conduction loss in the resonance process, external anti-parallel Schottky diodes with low forward voltage drop are used. The primary MOSFETs of each equalizer unit adopt two half bridge drive chips LM25101 with four optocouplers TLP117 for isolation switch drive. The secondary side output switch is driven by an optocoupler TLP152 directly. Schottky diode TMBAT49 with sufficiently large rated current, relatively small junction capacitance and forward voltage drop is selected as the secondary side rectifier diode. The PCB of the equalizer is made of 2oz copper thickness. The selection table and important parameters of other components except resonant inductor and resonant capacitor are shown in Table III.

TABLE III
COMPONENTS SELECTION TABLE

Circuit element	Type	Parameters
Primary side MOSFET	BUK7K8R7-40EX	$R_{on} \leq 8.5$ mΩ, $C_{oss} = 282$ pF
Primary side anti-parallel diode	DFL130L	$C_j = 76$ pF, $V_D \leq 0.36$ V
Secondary side output MOSFET	IPT007N06 N	$R_{on} = 0.75$ mΩ
Secondary side optocoupler	TLP152	The maximum delay is 190 ns
Secondary side rectifier diode	TMBAT49	$C_j = 35$ pF, $V_D \leq 0.42$ V
Current monitoring chip	INA181A3	Gain = 100, Bandwidth = 150 kHz

The sampling resistance of cell current and primary side resonant current is 10 mΩ, and the sampling resistance of secondary side output current is 50 mΩ. Current waveform is amplified by the current monitoring chip INA181A3, then tested by the oscilloscope or input into the isolated amplifier for ADC sampling. Their design positions are shown in Fig. 20.

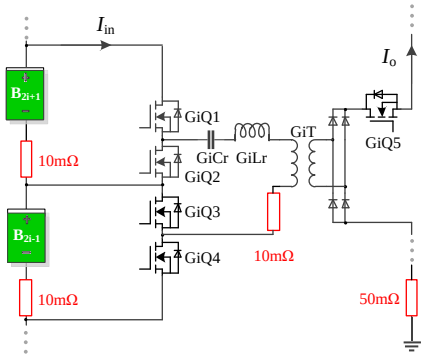


Fig. 20. Design position of primary and secondary current sampling resistor.

B. The Transformers and Resonant Components of Equalizer Units

Transformers of 3 equalizer units all use E18 paired with PLT18 planar magnetic cores of Ferroxcube Co., Ltd. The primary coil is designed as 2 turns and the secondary coil is 16 turns.

The operating magnetic flux intensity ΔB with 3.6 V input voltage, 50% duty cycle and 50 kHz switching frequency is calculated as 0.2 T, whereas the saturation magnetic flux density is 0.34 T. Transformer, resonant inductance and resonant capacitance parameters of 3 equalizer units are measured by the LCR tester Agilent E4980 A at a frequency of 50 kHz, as shown in Table IV.

TABLE IV
TRANSFORMER, RESONANCE INDUCTOR AND RESONANCE CAPACITOR PARAMETERS' MEASUREMENT VALUES

Resonance parameters		Value		
		G1	G2	G3
L_m		11.69 μH	11.71 μH	11.58 μH
L_f		0.22 μH	0.23 μH	0.23 μH
Comb. 1	L_r	1.43 μH	1.41 μH	1.38 μH
	C_r	1.49 μF	1.52 μF	1.56 μF
Comb. 2	L_r	6.93 μH	6.68 μH	6.71 μH
	C_r	0.83 μF	0.87 μF	0.86 μF

C. LLC Mode Normalized DC Voltage Gain Maximum Operating Point Test

The normalized DC voltage gain maximum point frequency is tested on each unit of the prototype. The test method is to start from the calculation value of the maximum point frequency based on (21), sweep the operation frequency of each unit under different initial values of M in increments of 1 kHz. Then, through the oscilloscope TPS2024, voltage waveforms of the primary switches are observed to judge whether each unit enters the ZVZCS state. Thus, the approximate value of the maximum point frequency is obtained. Efficiency and power component of equalizer unit at maximum point frequency is calculated and measured based on the measurement function of the oscilloscope. Characteristic test results are shown in Fig. 21, and power loss breakdown results are shown in Fig. 22.

From Fig. 21(a) and (b), it can be found the maximum M point of the three equalizer units has basically the same frequency change trend as in Fig. 12, but the frequency value needs to increase a certain float according to the theoretical value. The frequency curves of the three units are stored in the MCU of the switching signal source module to perform closed loop control on the LLC mode. As shown in Fig. 21(c) and (d), when the value of M decreases, the average equalizing current of the equalizer unit gradually increases. It leads to an increase in energy consumption including conduction loss. Therefore, energy efficiency of the equalizer unit decreases as the M value decreases in Fig. 21(e) and (f). By comparing Fig. 21(e) and (f), energy efficiency of Comb. 1 equalizer unit under different M values is always higher than of Comb. 2 equalizer unit. The energy efficiency of Comb. 1 is up to 88.73%, and the energy efficiency of Comb. 2 is up to 84.99%. This is

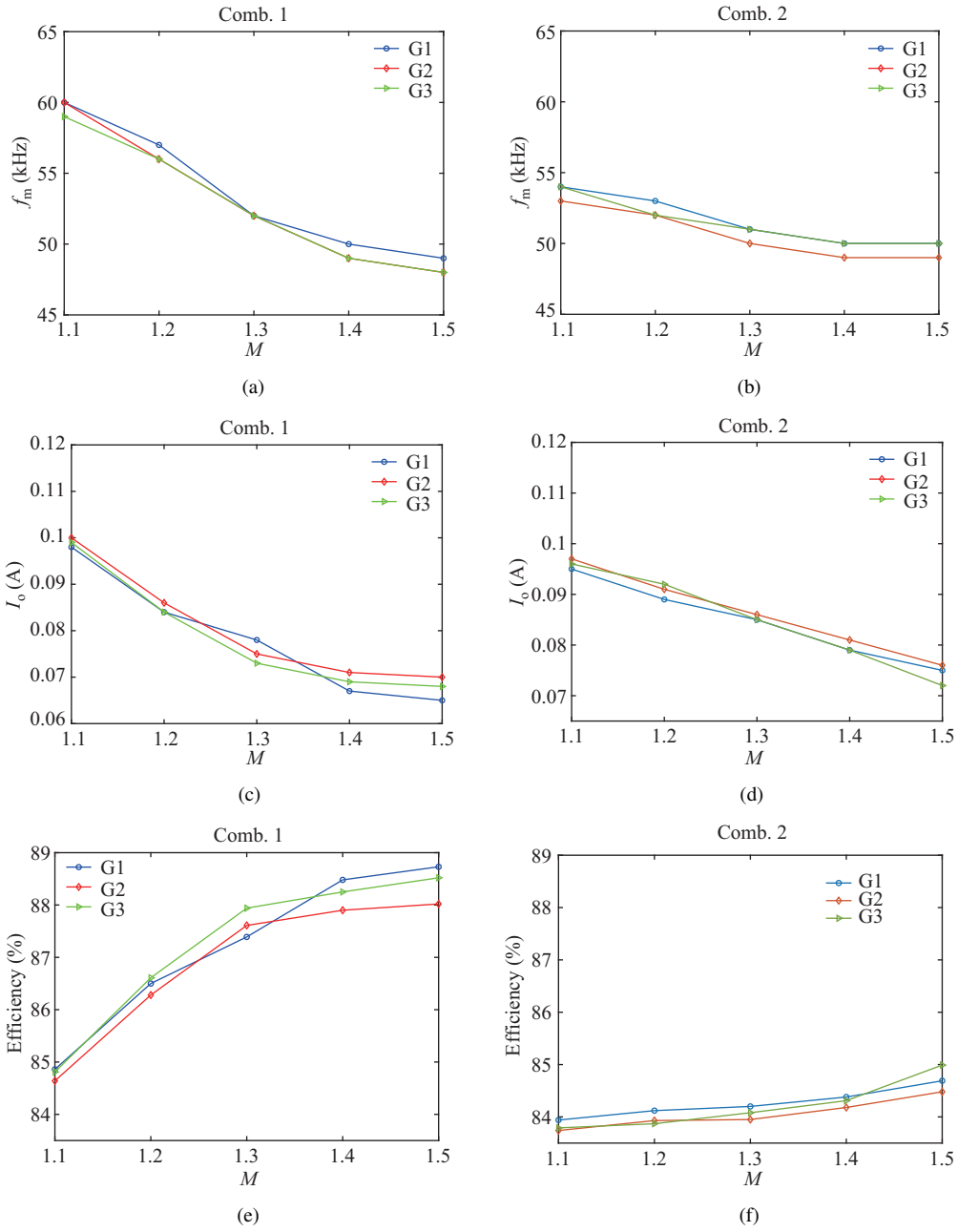


Fig. 21. The characteristic curve of normalized DC voltage gain maximum operating points under different M values. (a) f_{m} under Comb. 1. (b) f_{m} under Comb. 2. (c) Average output current I_{o} under Comb. 1. (d) I_{o} under Comb. 2. (e) Efficiency under Comb. 1. (f) Efficiency under Comb. 2.

because the Comb. 2 equalizer unit has a higher equalizing current, as shown in Fig. 21(c) and (d), and the larger series resonant inductor also results in an increase in DC impedance. By comparing Fig. 21(c) and (d), it can be observed that when the initial value of M is larger, the Comb. 2 equalizer unit has a larger equalizing current and faster equalization speed, whereas the Comb. 1 equalizer unit will gradually match or even surpass the Comb. 2 equalizer unit after the initial M value is greatly reduced.

Under different M values, the power breakdown when the equalizer operates at the maximum M value point of LLC mode is shown in Fig. 22. In Fig. 22, the total height of each column is the total input power of an equalizer unit. The method of adjusting M value in this test is to adjust the output battery pack voltage by fixing the input cell voltage. As can be seen from Fig. 22, since the LLC mode achieves ZVZCS state, the primary switching loss of the equalizer unit is very small and further decreases with the decrease of M value (just the output voltage value). As for the primary side conduction loss, since Comb. 2's primary side current in most cases is larger, Comb. 2 is larger than Comb. 1 in this term. The loss of transformer is affected by both operating current and switching frequency together, its change trend is not obvious. Finally, the secondary side loss will increase with the increase of output equalization current.

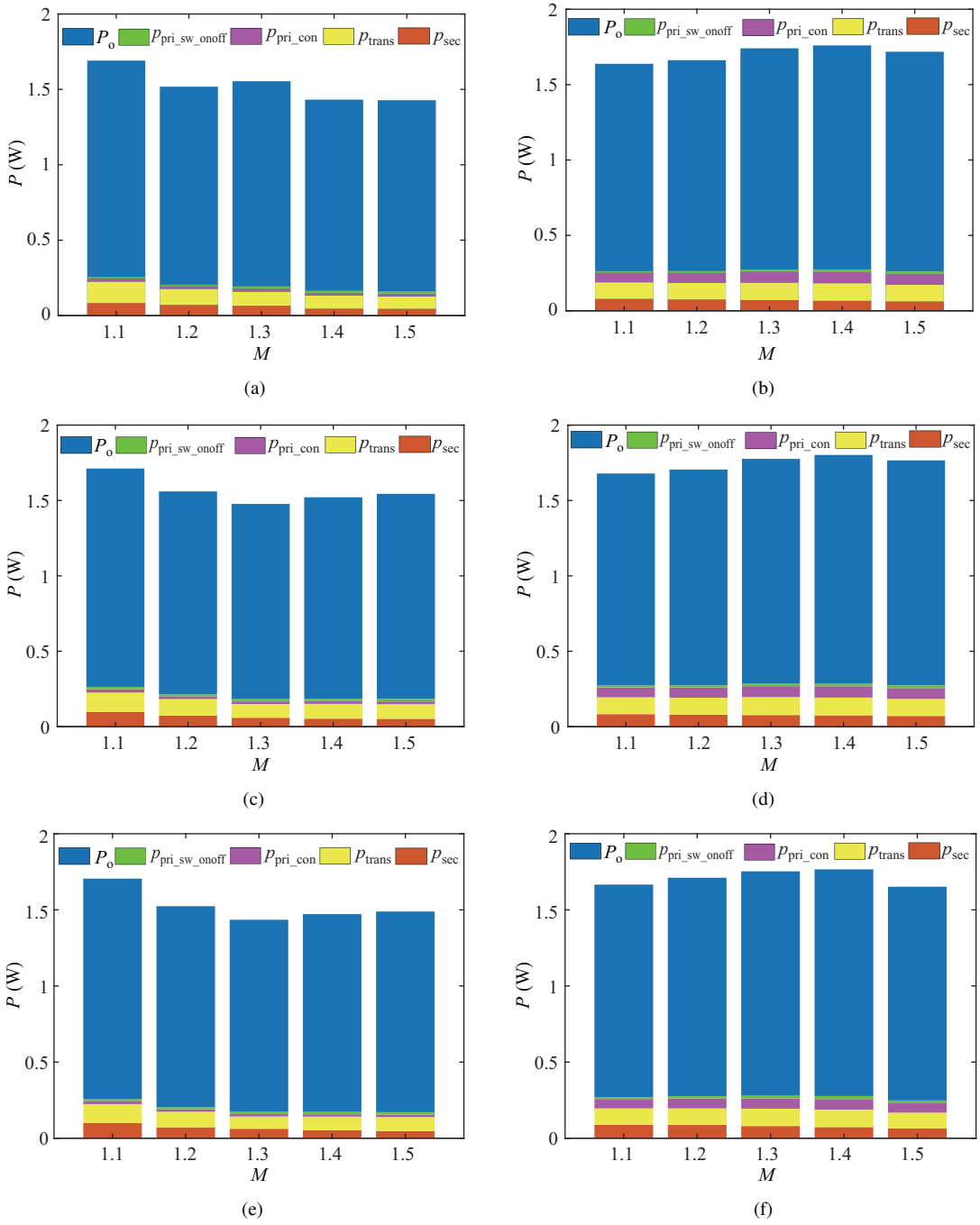


Fig. 22. Power breakdown for G1 to G3 equalizer units under different M values. (a) Unit G1 under Comb. 1. (b) Unit G1 under Comb. 2. (c) Unit G2 under Comb. 1. (d) Unit G2 under Comb. 2. (e) Unit G3 under Comb. 1. (f) Unit G3 under Comb. 2.

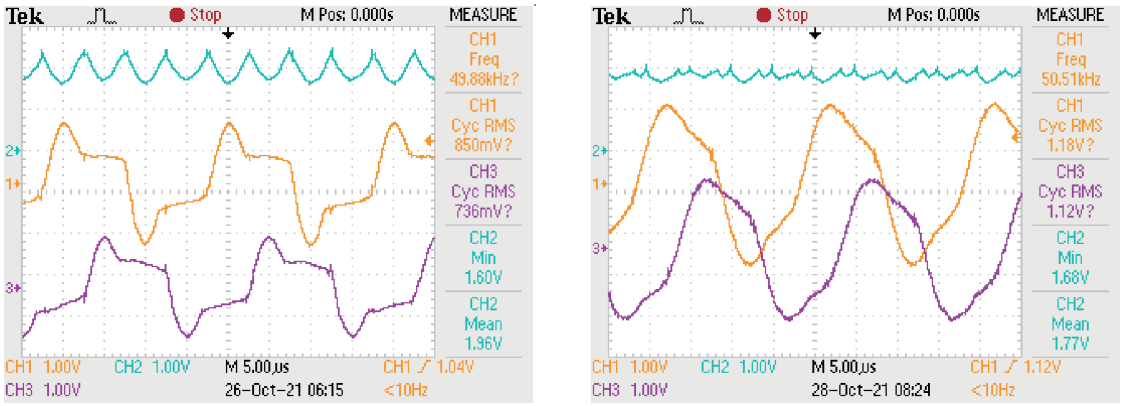
D. The Experiment of Interleaved Parallel LLC Resonance Mode

The main unit is the G1 unit, the slave unit is the G2 unit, the initial voltage of the donor cell in the G1 unit is 3.3 V, the initial voltage of the donor cell in the G2 unit is 3.26 V, and the initial voltage of the battery pack is 19.5 V. The two resonance parameters Comb. 1 and Comb. 2 are tested, respectively. The primary side resonance current and secondary side total current waveforms of the two equalizer units, as well as the driving signal and voltage waveform of the primary side MOSFETs are shown in Figs. 23–25.

In Fig. 23(a) and (b), the waveforms of CH1 are the primary resonance currents in interleaved parallel LLC master equalizer units with different parameters respectively, the waveforms of CH2 are the primary resonance currents in interleaved parallel LLC slave equalizer units, the waveforms of CH3 are both the secondary total output currents with different parameters. In Fig. 24(a) and (b), the waveforms of CH1 are the voltages of primary upper arm MOSFETs in interleaved parallel LLC master units, the waveforms of CH3 are the voltages of primary upper arm MOSFETs in interleaved parallel LLC slave units, and the waveforms of CH2 and CH4

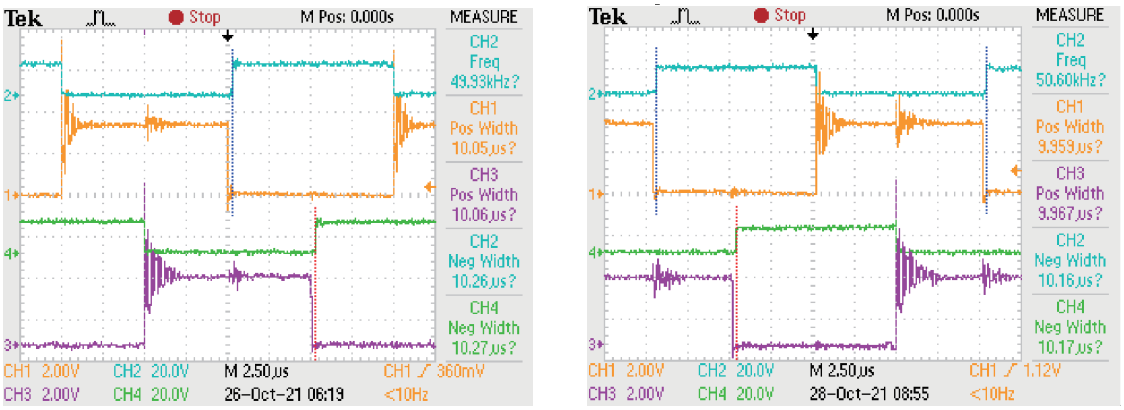
are their driving signal, respectively. Fig. 25 shows the related waveforms of the lower arm switches of the master and the slave unit, and their channel distribution in oscilloscope is basically the same as that in Fig. 24. In Fig. 26(a) and (b), the waveforms of CH1 are both the resonant currents of 3-state LC mode, the waveforms of CH2 are both the resonant capacitor voltages of 3-state LC mode.

In Fig. 23(a) and (b), since the setting position of the sampling resistance in Fig. 20, the waveform of the secondary side current is inverted with a 2.5 V DC bias voltage output from INA181A3, whereas the primary side resonant circuit is positive, which is presented in the AC mode of the oscilloscope. By comparing Fig. 15 with Fig. 23, the effect of the interleaved parallel method to limit the ripple



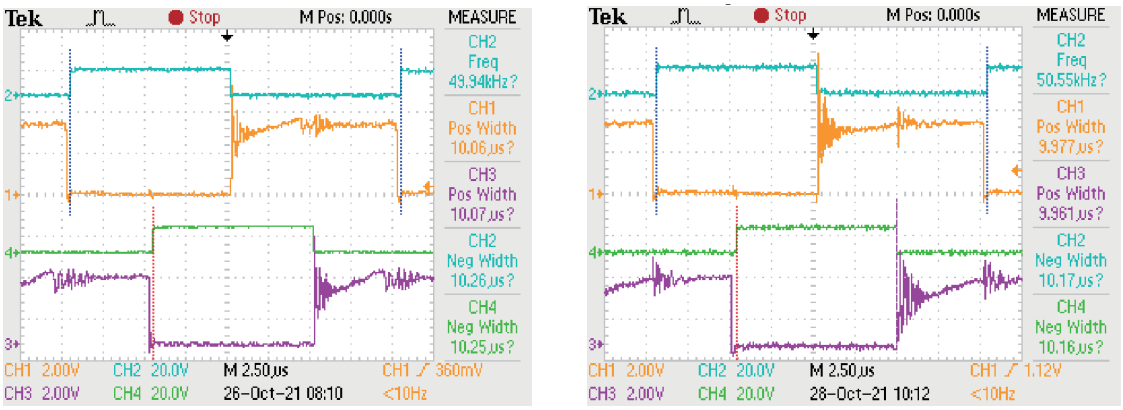
(a) (b)

Fig. 23. The primary side resonance current and secondary side total current in interleaved parallel LLC mode. (a) Comb. 1. (b) Comb. 2.



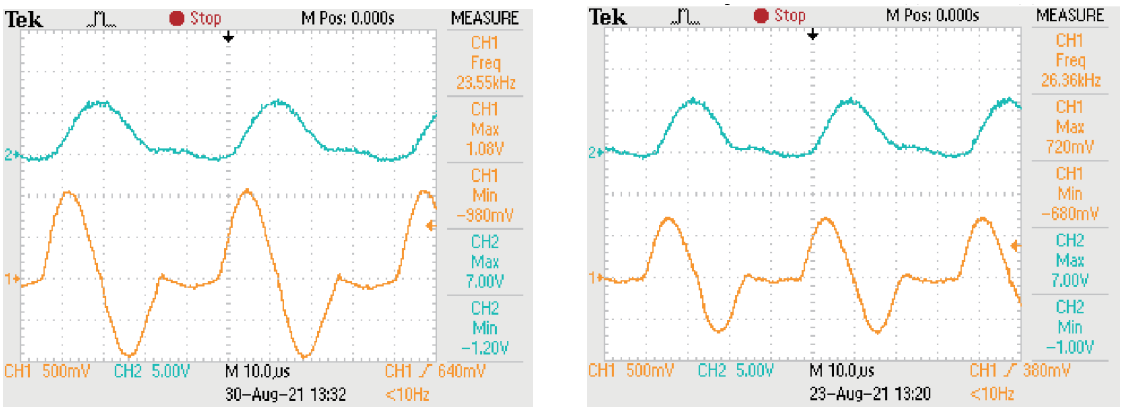
(a) (b)

Fig. 24. The driving signal and voltage waveform of primary side upper arm switch in interleaved parallel LLC mode. (a) Comb. 1. (b) Comb. 2.



(a) (b)

Fig. 25. The driving signal and voltage waveform of primary side lower arm switch in interleaved parallel LLC mode. (a) Comb. 1. (b) Comb. 2.



(a) (b)

Fig. 26. The quasi-resonant current and capacitor voltage waveforms in 3-state LC quasi-resonance mode. (a) Comb. 1. (b) Comb. 2.

of the secondary side total current is verified by staggering the secondary side currents' peaks of the two equalizer units. By comparing Fig. 23(a) and (b), it can be found that Comb. 2 is able to obtain a smaller ripple of the secondary side total current. By observing Fig. 24(a) and (b), and Fig. 25(a) and (b), it can be seen that the master and slave equalizer units in interleaved parallel LLC mode can both achieve ZVS turn-on of the primary switch. Meanwhile, waveforms of the primary side resonant current show the time intervals in Fig. 23(a) and (b) are both shorter than half a cycle, which are occupied by the current peak when the transformer is clamped by the battery pack voltage. No matter Comb. 1 or Comb. 2, the working frequency of both units has not reached the resonant frequency. Therefore, the secondary side diode of master and slave unit can also realize ZCS separately.

E. The Experiment of 3-state LC Quasi-resonance Mode

After the secondary side output switch is turned off, the 3-state LC mode experiment is performed. The initial voltages of the donor cell and the acceptor cell are both 3.3 V. The waveforms of the quasi-resonant current and capacitor voltage are shown in Fig. 26.

Figure 26 verifies the effect of the 3-state LC mode to achieve ZVG equalization. By observing the waveform changes of Comb. 1 and Comb. 2 capacitor voltages, it can be seen that in the third state of quasi-resonance, the capacitor voltage can fall back to a negative value. It means the preparation for the rapid discharge of the donor cell in the next cycle has been completed. After being measured by oscilloscope TPS2024, the quasi-sinusoidal positive half wave current peak value in Comb. 1 quasi-resonance's first state is converted to 1.08 A, the quasi-sinusoidal negative half wave current peak value in Comb. 1 quasi-resonance's second state is converted to 0.98 A. The quasi-sinusoidal positive half wave current peak value in Comb. 2 quasi-resonance's first state is converted to 0.72 A. After removing spikes at the current peak, the quasi-sinusoidal negative half wave current peak value in Comb. 2 quasi-resonance's second state is converted to 0.66 A. As a result, in the 3-state LC mode, the efficiency of Comb. 1 is about 90.7%, the efficiency of Comb. 2 is about 91.7%. The efficiency of Comb. 2 is slightly higher than of Comb. 1, but the equalization speed of Comb. 2 is much slower.

F. The Test of the SOC Based Equalization Scheme Selection Strategy

The system uses ampere hour integration (coulomb counting) method [33] to estimate the real-time SOC data of each cell. The coulombic efficiency of each cell is uniformly set to 99%. The battery pack and cell state ADC module record one data point every 0.9 s. Under the same cell initial state, the three different equalization tests are carried out by aforementioned Comb. 1 equalizer. Each cell should stand for 1 hour after constant current discharge, before being used for these tests. The initial SOC values of cells B1 to B6 are 75%, 72%, 69%, 66%, 63%, and 60%, respectively. During the charging and discharge test, the battery pack is charged and discharged at a constant current of 0.25 A separately. The charge device is GWinstek PPE-3323, and the discharge device is ITECH IT8513B.

In the three equalization tests, the working process of the equalizer is basically the same, as shown in Fig. 27. At the beginning of the test, equalizer units G1 and G2 work in interleaved parallel LLC mode, and cell B1 and B3 are used as donor cells. The equalizer unit G3 works in the 3-state LC mode, with cell B5 as the donor cell and cell B6 as the acceptor cell. In about 4∼5 minutes, the SOC curves of cells B5 and B6 first converge, and unit G3 then enters the standby state. Right after that, the SOC curves of cells B1 and B2 converge followed by the SOC curves of cells B3 and B4. Thereafter, in G1 unit, cells B1 and B2 are used as LLC mode's donor cells in turn, and in G2 unit, cells B3 and B4 operate the same way. In about 23 minutes, the SOC curves of cells B1, B2, B3 and B4 gradually converge. After that, the equalizer unit G2 exits the LLC mode and remains on standby, while the equalizer unit G1 still operates in the LLC mode until the SOC curves of all cells converge.

In the static equalization test, the difference between the SOC value of all cells and the average SOC value of the whole battery pack is reduced to less than 0.1% in about 43 minutes 26 seconds. The equalizer takes about 42 minutes 27 seconds to complete the same effect in the charge equalization test,

and about 44 minutes 52 seconds to achieve the same effect in the discharge equalization test. The above results show that this equalizer can achieve faster speed in charge equalization.

VIII. Hardware Size and Performance Comparison

Table V illustrates a comprehensive comparison of the proposed equalizer with the existing single layer active solutions. Comparison in Table V focuses on hardware size, equalization speed (denoted by P1), efficiency (denoted by P2), control simplicity (denoted by P3), extendibility (denoted by P4), and impact on battery life (denoted by P5). Hardware size is evaluated by the number of main circuit components, by assuming the battery string has m cells connected in series. The components include MOSFET (denoted by MOS), relay (denoted by RE), diode (denoted by D), inductor (denoted by L), capacitor (denoted by C), single transformer (denoted by T), and multi-winding transformer (denoted by MT).

Performance from P1 to P5 are scored by "excellent (E)", "very good (VG)", "good (G)", "satisfactory (S)", and "poor (P)." When equalizer's speed is evaluated: a minute level time within 1 hour means VG or even higher; an hour level time within 2 hour means G; if the equalization time exceeds 2 hours, the score will not exceed S. When equalizer's efficiency is evaluated: an efficiency that consistently exceeds

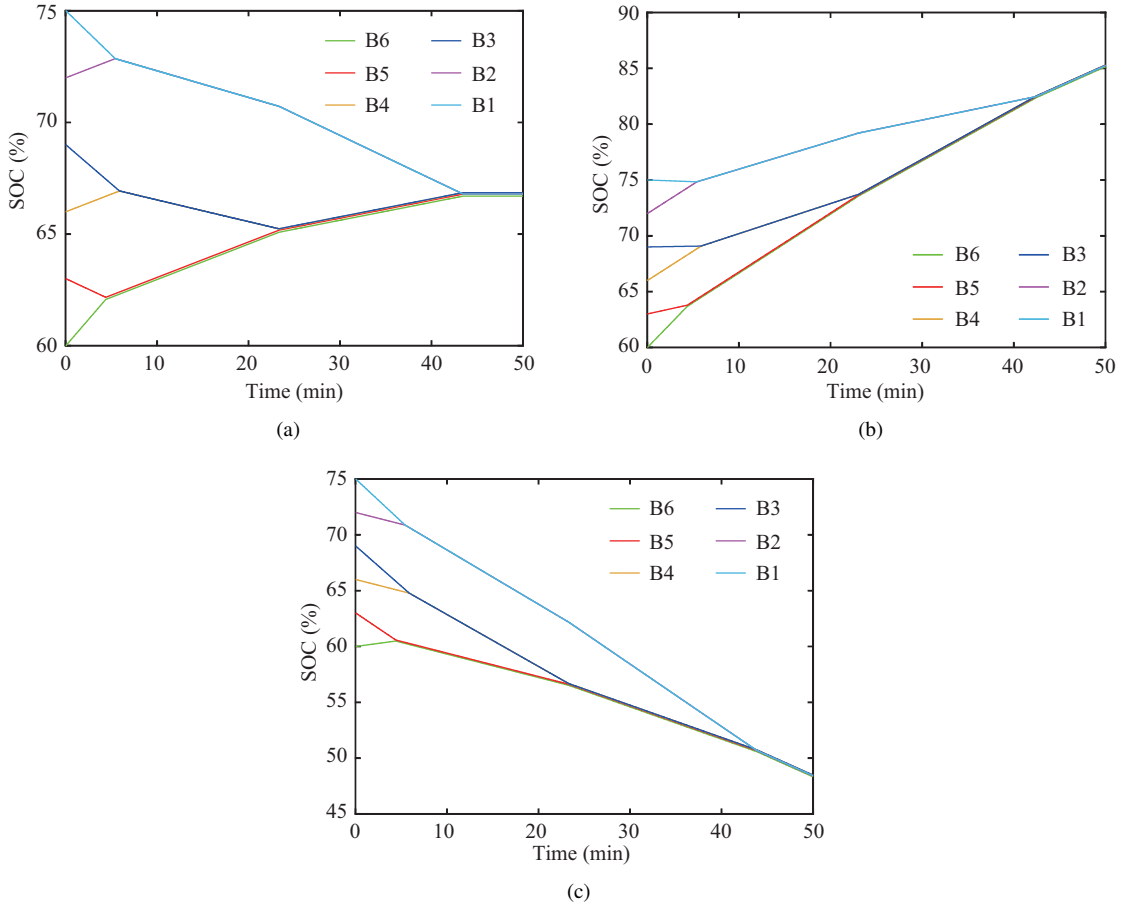


Fig. 27. SOC change curve of each cell in the equalization test. (a) Static equalization. (b) 0.25 A charge equalization. (c) 0.25 A discharge equalization.

TABLE V
Comparison of Different Single Layer Active Equalizers in Teams of Hardware Size and Performance

Equalizer	Number of main circuit components							Performance				
	MOS	RE	D	L	C	T	MT	P1	P2	P3	P4	P5
3-state resonator ACTC [5]	$5(m-1)$	0	0	$m-1$	$m-1$	0	0	G	VG	VG	S	P
Cuk conv. ACTC [6]	$2(m-1)$	0	0	$2(m-1)$	$m-1$	0	0	E	VG	S	VG	P
Multiphase conv. ACTC [22]	$2(m-1)$	0	0	$m-1$	0	0	0	S	E	VG	VG	P
LLC resonator DCTC [7]	$4(m+2)$	2	2	1	1	1	0	VG	E	VG	S	G
Matrix LC conv. DCTC [24]	8	$4m$	0	1	1	0	0	VG	VG	G	G	P
Switch array CTP [12]	$2(m-1)$	0	$2m-1$	0	0	1	0	G	S	VG	G	P
Multi-transformers PTC [15]	2	0	$4m$	0	0	m	0	E	G	E	G	G
Multi-winding PTC [17]	$2m$	0	0	0	0	0	1	VG	E	G	P	P
Integrated cascade conv. CTP/PTC [18]	$2(m+5)$	0	0	2	3	1	0	G	G	G	E	E
Proposed Equalizer	$2.5m$	0	$2m$	$0.5m$	$0.5m$	$0.5m$	0	E	VG	G	VG	E

P1: Speed; P2: Efficiency; P3: Control simplicity; P4: Extendibility; P5: Impact on battery life.
E: Excellent; VG: Very Good; G: Good; S: Satisfactory; P: Poor.

90% means E; an efficiency that will vary from 80% to no more than 95% with the operation state means VG; an efficiency that will vary from 75% to no more than 90% means G; an efficiency that will vary from 70% to no more than 85% means S; if the efficiency is always below 80%, the score is P. The equalizer's control simplicity is evaluated by integrating the complexity of control algorithm, the number of feedback signals and switch driving signals. The equalizer's extendibility is evaluated by integrating the degree of modularity, difficulty in making transformers, switches and energy components number. For example, 3-state resonator equalizer in [5] has excellent degree of modularity, but it has too many switches, so the extendibility score is only S. The proposed equalizer's switches number is only $2.5m$. If some efficiency is sacrificed, the secondary output switch GiQ5 of every unit can be replaced by relay. This means the switches number can be further reduced to $2m$. In addition, its single transformers number is also less than the traditional multi-transformers topology in [15]. Therefore, the proposed scheme still has very good extendibility. The proposed equalizer is especially suitable for the current situation of tight IC chip supply. Finally, the evaluation index of equalizer's impact on battery life is whether the equalizer can output continuous equalization current and whether it has effective control of the equalization current ripple. The proposed equalizer and the equalizer based on integrated cascade converter in [18] have the above characteristics. The equalizer based on LLC resonator in [7] and the multi-transformers equalizer in [15] both have critical continuous equalization current, but they do not have the ability of ripple control.

An intuitive performance comparison is drawn, as shown in Fig. 28, by selecting the optimal existing topologies in Table V belonging to five different equalization types together with the proposed equalizer.

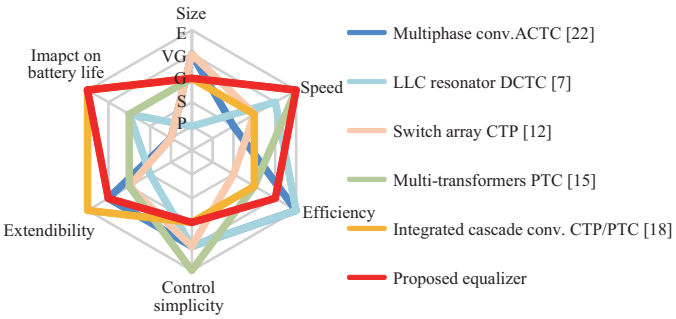


Fig. 28. Comparison of different single layer active cell equalizers.

In general, the comparison results further show the superiorities of the proposed equalizer in terms of switches number, speed, efficiency, extendibility, and impact on battery life.

IX. Conclusion

This paper proposes a mode-varying cell equalizer which combines the advantages of CTP and ACTC structures. Every unit of the equalizer can freely switch between LLC mode and 3-state LC mode. Moreover, the number of transformer's total turns is reduced based on the boosting effect of LLC structure. When multiple units operate in LLC mode at the same time, interleaved parallel technology is used to limit secondary side current ripple. A closed loop LLC mode control algorithm based on secondary side output current and variable DC voltage gain is proposed to selectively turn on interleaved parallel mode and ensure the primary and secondary side circuits work in ZVZCS state. When the interleaved parallel mode is turned on, the ripple of multiple equalizer units' total output current is limited to the ripple of a single unit's output current. A SOC based equalization scheme selection strategy is designed to intelligently select the operating mode of each equalizer unit. The experimental prototype for 6 series battery under 2 combinations of resonance parameter is built. The frequency at the maximum point of the DC voltage gain, the efficiency and output current of every equalizer unit at this frequency are measured and analyzed. The circuit waveforms in interleaved parallel LLC mode and 3-state LC mode are obtained and analyzed comparatively. In LLC mode, the equalizer with resonance parameters Comb. 1 has higher efficiency in most cases, but the output current ripple is larger, whereas the equalizer with Comb. 2 has the opposite; and in 3-state LC mode, the equalizer with Comb. 1 has lower efficiency than the equalizer with Comb. 2. Static, charge and discharge equalization tests are performed to verify minute level equalization speed of the proposed equalizer. Finally, the advantages of the proposed equalizer are illustrated through a comprehensive comparison in hardware size and performance with the other 9 existing equalizers.

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