

Stability Limitations and Analytical Evaluation of Voltage Droop Controllers for VSC MTDC

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Abstract—This paper presents a systematic analysis of DC voltage stability of a multi-terminal VSC-HVDC (MTDC) system, with the emphasis on a comparative study of the most ubiquitous droop control configurations. The paper introduces a general framework for the analysis of various droop control configurations employed in MTDC systems. This framework is then used to compare leading droop control configurations in terms of their impact on the relative stability, performance and robustness of the overall MTDC system. A generalized analytical MTDC model that contains detailed models of AC and DC system components is derived. Limitations imposed by DC power flow, DC inductor, cable modeling and AC network impedance on DC system stability are identified. Classical and multivariable frequency response analysis and eigenvalue analysis are applied to open-loop and closed-loop models to compare the stability and robustness of five leading droop controllers, with the focus on feedback signal selection and controller parameterization. This paper also proposes an active stabilizing controller, which takes the form of a modified constant power control, to enhance the controllability and robustness of the DC voltage control.

Index Terms—VSC HVDC, MTDC control, stability, droop control, mathematical modeling.

I. INTRODUCTION

Voltage source converter (VSC) HVDC is a rapidly developing technology and has a great potential in future power systems for renewable energy integration and AC system reinforcement. Multi-terminal VSC-HVDC (MTDC) systems, which are likely to be developed gradually by interconnecting point-to-point links, are expected to offer enhanced reliability, flexibility and controllability.

In a MTDC system, DC voltage indicates the power balance and stability of the DC network. DC voltage control needs to be able to handle the fast electromagnetic dynamics of the DC network. Relying on fast telecommunications for DC system stabilization is generally considered to be unreliable, hence the DC voltage control of MTDC systems is likely to be based on local converter signals and employ a distributed architecture.

Droop control is recommended by a majority of previous literature for this kind of distributed control i.e. DC voltage and power sharing [1]–[6]. The basic idea of this control is to allow

multiple converters to simultaneously regulate their DC voltages by enabling a proportional steady-state droop relationship between the DC voltage and power/current. However the dynamic implementation of this control has not been standardized and the impact of the droop control structures on MTDC stability requires further analysis.

In order to analyze MTDC stability considering various types of DC voltage controllers, a generalized mathematical model including detailed AC and DC component models is required. A single converter or point-to-point system with constant DC voltage control is generally used for stability analysis of VSC-HVDC [7–11]. A number of previous papers regarding droop control have focused on the steady-state and dynamic simulation aspects [1, 3, 4, 6, 12, 13]. Stabilities of a single VSC converter model with several types of voltage droop structures are compared in [14]. Some good work exists investigating mathematical modeling and AC/DC interaction analysis of MTDC systems [5, 15], but none yet provides a comparative stability analysis of MTDC systems considering different droop implementations.

This paper primarily aims to address the key limitations imposed on MTDC stability, and comparatively evaluate the stability of MTDC systems with five ubiquitous types of DC voltage droop control structures. Another key contribution of this paper is to provide a generalized mathematical framework which is suitable for stability and robustness analysis of various DC voltage control controllers. Under this framework, classical and multivariable frequency response analysis and eigenvalue analysis are employed to investigate MTDC system stability. This paper also proposes an active stabilizing control to enhance the robust stability for MTDC systems installed with large reactors.

This paper is structured as follows. In Section II, a dynamic modeling framework that is suitable for DC voltage stability studies is presented. General constraints posed by DC power flow, DC inductor, cable modeling and AC system strength on droop control stability are analyzed in Section III. A comparative study of the leading droop controllers is performed in Section IV to identify specific limitations of the controllers. Finally, an active stabilizing controller is proposed to mitigate the negative impedance effect and improve robustness with respect to power flow.

II. ANALYTICAL MODELING

A generalized analytical modeling approach is presented in this section for the analysis of MTDC system stability.

Manuscript received July 1, 2016; revised December 16, 2016, 10 March, 2017; accepted June 15, 2017. This work was supported by the UK Engineering and Physical Science Council Project EP/L102463/1.

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DOI: 10.17775/CSEEJPES.2016.00670

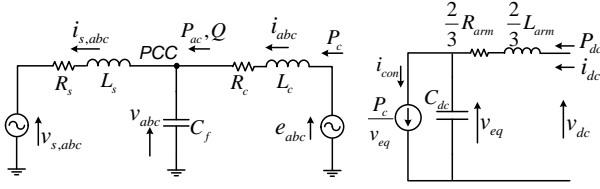


Fig. 3. Average-value model (AVM) for VSC-HVDC

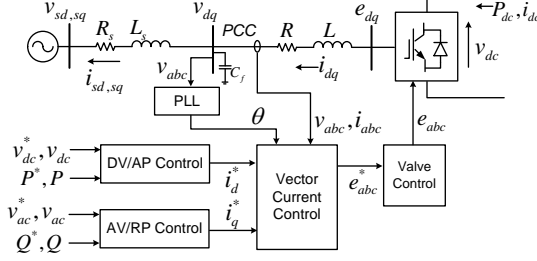


Fig. 4. VSC-HVDC control structure.

A. Converter System Modeling

The converter system model employed in this paper is primarily based on the average-value model (AVM) developed in [16] and [17] for modular multilevel converters (MMC). As depicted in Fig. 1, the converter AC terminal is modeled by a controlled voltage source interfacing with the point of common coupling (PCC) through a lumped impedance representing both transformer and arm impedances. The AC system strength is quantified by the short-circuit ratio (SCR) which is directly linked to the system impedance. The converter DC side is modeled by a controlled DC current source based on the power balance principle. An equivalent DC capacitance C_{dc} is computed based on the derivations presented in [18]. The arm inductor is also modeled on the DC side, since one third of the DC current flows through the arm inductor in each phase [16].

As shown in Fig. 2, a cascaded control system for VSC-HVDC is typically implemented in a dq synchronous frame, where the transformation angle is provided by a phase-locked loop (PLL). The active current reference is provided by a DC voltage (DV) controller or an active power (AP) controller. The AC voltage or reactive power is controlled by manipulating the reactive current.

B. Candidate Droop Controllers

According to existing literature (see below), dynamic implementations of the DC voltage droop controller can be classified into five types that are depicted in Fig. 3. These designs aim to achieve similar or identical steady-state voltage droop characteristics. The droop constant K_{dr} , which is interpreted here as the ratio between the steady-state deviation of DC voltage to change in ac or DC power, is likely to be selected primarily based on power flow requirements in terms of power sharing and DC voltage deviation [3, 4, 6, 13].

The Type 1 model has been widely used in previous literature [2, 5, 19], where the V - P_{ac} droop characteristic is realized by modifying the active power reference in proportion to the DC voltage error. The Type 1 droop control effectively acts as the outer control of the active power control. Alternatively, as shown in Type 2, V - P_{ac} droop can be achieved by modifying the standard DV controller using a supplementary signal in proportion to the active power error [3].

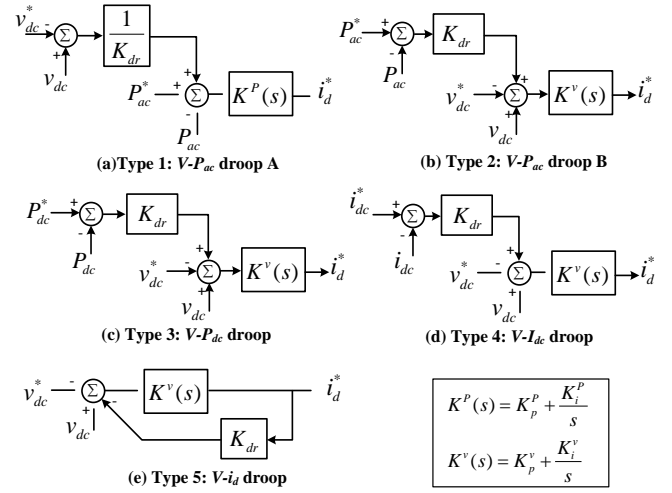


Fig. 1. Five types of dc voltage droop control implementations.

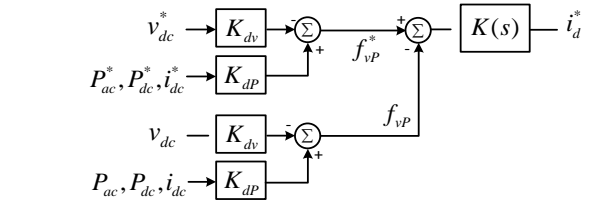


Fig. 2. Generalized droop control structure.

TABLE I
DROOP CONTROLLER PARAMETERS OF TYPES 1-5

Parameters	Type 1	Type 2	Type 3	Type 4	Type 5
K_{dv}	$1/K_{dr}$	1	1	1	1
K_{dp}	1	K_{dr}	K_{dr}	K_{dr}	0
$K(s)$	$K_p^p + \frac{K_i^p}{s}$	$K_p^v + \frac{K_i^v}{s}$	$K_p^v + \frac{K_i^v}{s}$	$K_p^v + \frac{K_i^v}{s}$	$\frac{1}{K_{dr}} \frac{Ts+1}{\beta Ts+1}$

In Type 3 and Type 4, DC power or DC current imported by the converter is used to produce the supplementary signal for the DV controller adjustment to obtain V - P_{dc} or V - I_{dc} droop respectively [1, 4, 13]. These two types are of particular interest if system operators are more concerned with DC rather than ac power flow.

Type 5 is derived based on the frequency droop concept that droop control can be obtained by adding a proportional feedback loop around the main controller [20]. This implementation is very similar to the standard design for generator governors and STATCOM controls; however it has rarely been discussed for MTDC applications. One possible drawback of this design is that specified V - P droop characteristics cannot be perfectly achieved by Type 5 due to the mismatch between the active power and d -axis active current.

C. Generalized Droop Controller Modeling

The droop implementations and typical AP or DV controllers described in Section II B can all be represented in the generalized form shown in Fig. 4. A new droop variable f_{vp} , which is defined as the sum of the DC voltage multiplied by DV droop gain K_{dv} and AC/DC current/power multiplied by AP droop gain K_{dp} , is considered as the new output signal to be

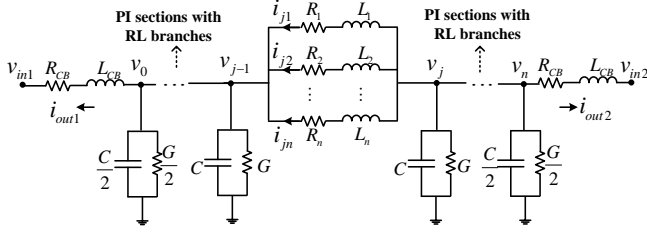


Fig. 5. Cable model with parallel RL branches.

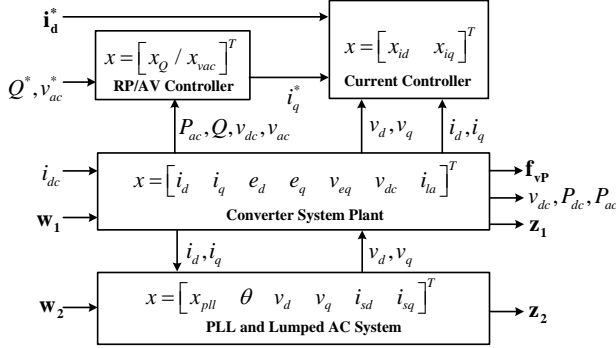


Fig. 6. State-space VSC model for DV/AP control studies.

controlled in order to have a zero steady-state error. As shown in Table I, the DV and AP droop gains K_{dv} and K_{dp} are related to the slope K_{dr} as: $K_{dr} = K_{dp}/K_{dv}$. The main controller $K(s)$ is normally a PI controller for typical droop schemes but a more complex controller can be easily incorporated in this generalized droop structure.

This generalized droop control structure shown in Fig. 4 enables various types of DV/AP controllers to be evaluated under a common framework. A similar control structure is also applicable to the general representation of a constant ac voltage control, reactive power control and droop AC voltage control. Furthermore, functionality and flexibility of the mathematical modeling of MTDC systems are also greatly improved by utilizing this control topology.

The DV controller $K^D(s)$ and AP controller $K^P(s)$ presented in Fig. 3 are typically PI controllers. The superscripts ‘v’ and ‘P’ denote whether the related PI controllers are designed based upon the DC voltage plant or the active power plant respectively. Please note that per unit representation is used throughout this paper.

The PI AP controller $K^P(s)$ can be tuned using the Skogestad internal model control (SIMC) method [21]:

$$K_p^P = \frac{\tau_{id}}{\tau_{des}}, \quad K_i^P = \frac{1}{\tau_{des}} \quad (1)$$

where τ_{id} is the time constant of the d -axis current loop and τ_{des} is the desired time constant of the AP control loop.

SIMC can also be applied for the tuning of the PI DV controller and the resulting parameters are:

$$K_p^v = \frac{C_{dc}}{\tau_{des} + \tau_{id}}, \quad K_i^v = \frac{C_{dc}}{4(\tau_{des} + \tau_{id})^2} \quad (2)$$

where C_{dc} is the equivalent DC link capacitance and τ_{des} is the desired time constant of the DV control loop. For similar closed-loop bandwidth, the proportional gain in the DV controller $K^v(s)$ is usually much larger than the proportional gain in the AP controller $K^P(s)$, since at low frequencies the AP

plant model is dominated by a large steady-state gain whereas the DV plant model is dominated by an integrator.

Type 5 controllers can be shown in the generalized droop control structure with $K(s)$ represented as a lag compensator:

$$K(s) = \frac{1}{K_{dr}} \cdot \frac{Ts + 1}{\beta Ts + 1}, \quad \text{where } T = \frac{K_p^v}{K_i^v}, \quad \beta = 1 + \frac{1}{K_p^v K_{dr}}. \quad (3)$$

D. Cable Modeling

The cascaded π -section cable (CPIC) model is commonly adopted for mathematical modeling of VSC-HVDC systems [5, 8, 22]. However, as identified in [11], relying on the CPIC may give false judgement of DC system stability since the resistance of the CPIC model can be much lower than that of a frequency-dependent (FD) cable model [23]. Therefore, a modified π -section cable (MPIC) model proposed in [11] is utilized here for state-space modeling of DC lines to give a more accurate representation of DC system dynamics. In the MPIC model shown in Fig. 5, each π section is comprised of multiple parallel RL branches to provide a degree of frequency-dependency. For a symmetrical monopole system, based upon the FD cable model in PSCAD/EMTDC, frequency scan results of the series impedance of both positive and negative poles are employed to account for the mutual impedance. Vector fitting is utilized for the parameterization process [24].

A DC inductor L_{CB} , which is required by DC circuit breakers for fault current limiting, is included at both ends of each cable as shown in Fig. 5. A state-space model of a cable model that consists of n parallel branches and m π sections has $(mn+m+3)$ state variables.

E. Open-Loop and Closed-Loop Models

This section briefly describes the open-loop and closed-loop formulations of a generalized small-signal MTDC model.

All the differential equations which describe the dynamics of ac and DC systems, converters and controllers need to be identified and linearized around a specified operating point, which is provided by a power flow calculation. Detailed derivations of these linearized equations are provided in [19, 22]. The open-loop VSC system model used to assess DV/AP control structures is formulated by interconnecting multiple sub-systems, as illustrated in Fig. 6, where x_Q and x_{vac} represent the states of the RP and AV controllers respectively; the states of the PI current controllers are denoted by x_{id} and x_{iq} ; the state of the PLL loop filter is denoted by x_{pll} ; θ is the output angle of the PLL; and the notation of the states related to converter ac and DC plants are shown in Fig. 1 and Fig. 2. In Fig. 6, w_1 and w_2 represent exogenous input vectors, whereas z_1 and z_2 are exogenous output vectors.

In a MTDC system, a general state space model for the j th VSC system can be written as, where x_j and u_j are the state variables and the input vector of the j th converter respectively. The DC current injected into the j th converter $i_{dc(j)}$ and the converter DC voltage $v_{dc(j)}$ are treated separately from other inputs/outputs, since converter models and the DC network models are integrated together through the exchange of DC voltages and currents.

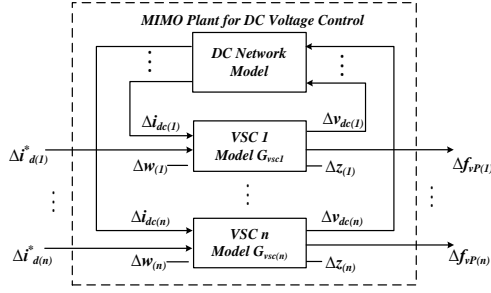


Fig. 8. Open-loop MTDC model for dc voltage control studies.

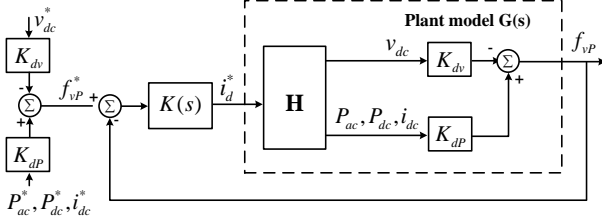


Fig. 9. SISO closed-loop diagram for the generalized DV/AP control.

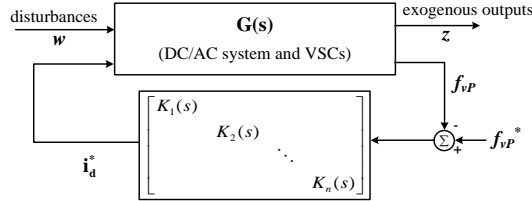


Fig. 10. Closed-loop diagram for DC voltage control.

$$\begin{aligned} \dot{\mathbf{x}}_j &= \mathbf{A}_j \mathbf{x}_j + \begin{bmatrix} B_{jG} & B_j \end{bmatrix} \begin{bmatrix} i_{dc(j)} \\ \mathbf{u}_j \end{bmatrix} \\ v_{dc(j)} &= C_{jG} \mathbf{x}_j \\ \mathbf{y}_j &= C_j \mathbf{x}_j + \begin{bmatrix} D_{jG} & D_j \end{bmatrix} \begin{bmatrix} i_{dc(j)} \\ \mathbf{u}_j \end{bmatrix} \end{aligned} \quad (4)$$

The state-space model of the overall DC network is formed by aggregating all the cable models and it can be written as:

$$\begin{aligned} \dot{\mathbf{x}}_G &= \mathbf{A}_G \mathbf{x}_G + \mathbf{B}_G \mathbf{v}_{dc} \\ \mathbf{i}_{dc} &= \mathbf{C}_G \mathbf{x}_G. \end{aligned} \quad (5)$$

For a MTDC system with n terminals, by interconnecting the analytical models of all the converter systems in the form of and the DC network model in the form of , the overall state-space model is given as:

$$\begin{aligned} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \\ \vdots \\ \dot{\mathbf{x}}_n \\ \dot{\mathbf{x}}_G \end{bmatrix} &= \begin{bmatrix} \mathbf{A}_1 & 0 & \cdots & 0 & B_{1G} C_{G1} \\ 0 & \mathbf{A}_2 & \cdots & 0 & B_{2G} C_{G2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & \mathbf{A}_n & B_{nG} C_{Gn} \\ B_{G1} C_{1G} & B_{G2} C_{2G} & \cdots & B_{Gn} C_{nG} & \mathbf{A}_G \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \vdots \\ \mathbf{x}_n \\ \mathbf{x}_G \end{bmatrix} \\ &+ \begin{bmatrix} B_1 & 0 & \cdots & 0 \\ 0 & B_2 & & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \\ \vdots \\ \mathbf{u}_n \end{bmatrix} \end{aligned} \quad (6)$$

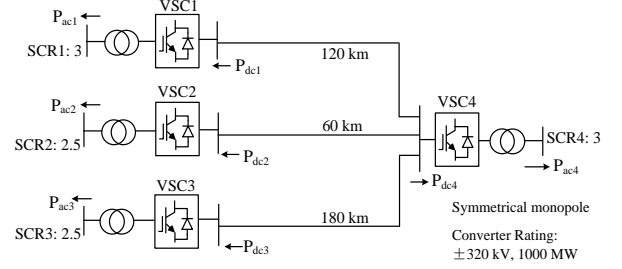


Fig. 7. Four-Terminal VSC MTDC test system.

Scenario	VSC1(p.u.)	VSC2(p.u.)	VSC3(p.u.)	VSC4(p.u.)
PF1	-0.750	-0.600	0.759	0.580
PF2	0.750	0.600	-0.781	-0.580

$$\begin{bmatrix} \mathbf{y}_1 \\ \mathbf{y}_2 \\ \vdots \\ \mathbf{y}_n \end{bmatrix} = \begin{bmatrix} C_1 & 0 & \cdots & 0 & D_{1G} C_{G1} \\ 0 & C_2 & & 0 & D_{2G} C_{G2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & C_n & D_{nG} C_{Gn} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \vdots \\ \mathbf{x}_n \\ \mathbf{x}_G \end{bmatrix} + \begin{bmatrix} D_1 & 0 & \cdots & 0 \\ 0 & D_2 & & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & D_n \end{bmatrix} \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \\ \vdots \\ \mathbf{u}_n \end{bmatrix} \quad (7)$$

where B_{Gj} is the j th column of the input matrix B_G , C_{Gj} is the j th row of the output matrix C_G , and the zeros are submatrices with appropriate dimensions. This modeling approach can be conveniently applied to suit different MTDC dynamic studies.

Fig. 7 shows the structure of the multi-input-multi-output (MIMO) plant model for the DC voltage control, which can be extracted directly from the overall state-space MTDC model. The vector \mathbf{w} represents the exogenous input vector which is comprised of the commands and disturbances, with the active current reference excluded. The vector \mathbf{z} represents the exogenous output vector which is comprised of all the output variables to be observed, with the DC voltage v_{dc} and the droop variables f_{vP} excluded.

From the single-input-single-output (SISO) perspective, the generalized droop controller can be connected with this plant model, as presented in the closed-loop block diagram in Fig. 8, where \mathbf{H} is the 2×1 transfer function matrix between v_{DC} , $P_{ac}/P_{DC}/i_{DC}$ as outputs and i_d^* as input. The plant model $G(s)$, the sensitivity transfer function $S(s)$ and the complimentary sensitivity $T(s)$ can be represented as:

$$G(s) = \frac{f_{vP}}{i_d^*}, \quad S(s) = \frac{1}{1 + K(s)G(s)}, \quad T(s) = \frac{K(s)G(s)}{1 + K(s)G(s)} \quad (8)$$

In Fig. 7 and Fig. 8, the DV and AP droop gains are considered as part of the plant model $G(s)$ to allow classical stability analysis to be conducted and to provide a more general framework for comparative droop control study.

Closed-loop MIMO representation of the DC voltage control problem is shown in Fig. 9. Constant DV and AP controls as well as various droop controls can all be incorporated within this framework. In this MIMO model, the droop control plant model $G(s)$ referred in this paper for the j th converter is the transfer function that relates the j th i_d reference as the input to the j th droop function f_{vP} as the output. It is important to note that the droop gains K_{dP} and K_{dV} are part of the plant model, which will greatly facilitate stability analysis.

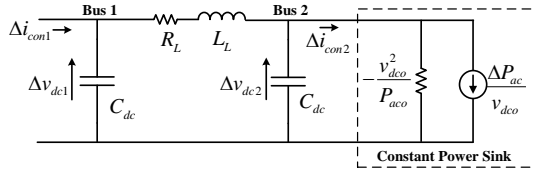


Fig. 11. Simplified dc link model with linearized DC power sink.

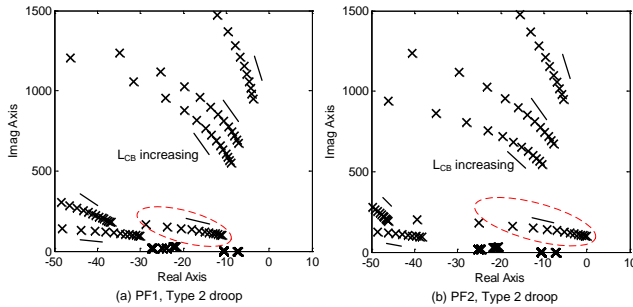


Fig. 12. Trajectories of selected closed-loop eigenvalues for scenarios PF1 and PF2 as the dc inductor varies from 0 to 150 mH (Type 2 droop, $K_{dr}=5\%$).

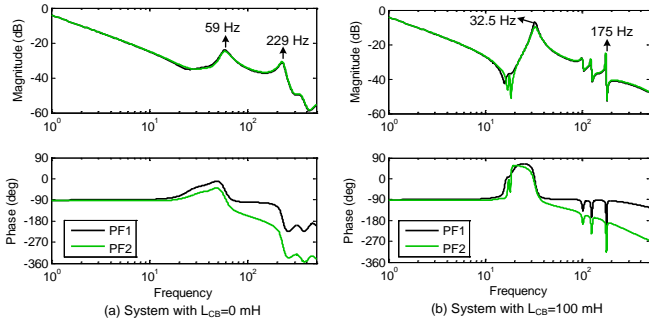


Fig. 13. Frequency responses of the open-loop transfer function $v_{dc1}(s)/i_{con1}^*(s)$, for systems with and without dc breaking inductor.

III. DC STABILITY LIMITATIONS

This section aims to address some key stability limitations that are independent from the droop control implementations. A four-terminal MTDC system schematically shown in Fig. 10 is used throughout this paper. Analytical models of this test system are built in MATLAB based on the methodology presented in Section II-E. A more accurate model using a FD cable model is built in PSCAD for time-domain simulations.

Two power flow scenarios, which are parameterized in Table II as PF1 and PF2, are used for all test cases. Inverter orientation ($P>0$ for inverters) and per unit values are used in this paper. VSC3 and VSC4 employ voltage droop control whereas active power control is applied to VSC1 and VSC2. The nominal value of the droop constant K_{dr} is 5%, for both VSC3 and VSC4. The nominal bandwidths of the DV and AP controllers are selected to be 18 Hz.

A. DC Inductor and DC Power Flow

DC circuit breakers rely on large DC inductors to limit the rise of the DC fault current. The DC inductor may however degrade the stability and transient performance of MTDC

systems [22, 25]. The detrimental effect caused by this component requires further in-depth analysis.

From the DC grid perspective, an inverter in constant power control can be approximated as a DC power sink. The DC current imported by this power sink can be linearized as:

$$i_{con} = \frac{P_{ac}}{v_{dc}} \Rightarrow \Delta i_{con} = \frac{\Delta P_{ac}}{v_{dco}} - \frac{P_{aco}}{v_{dco}^2} \Delta v_{dc} \quad (9)$$

where the subscript 'o' denotes the operating point. A DC link model shown in Fig. 11 is used to represent a simplified system and conceptually illustrate the impact of the DC inductor. An inverter in constant power mode behaves as a negative resistance in parallel with a DC current sink. The negative resistance will impose negative damping and reduce relative stability of the system. A similar effect has been analyzed in [26, 27] for DC links of low-power inverter drive systems.

For the generic DC link shown in Fig. 11, if the voltage v_{dc1} is to be controlled by varying the DC current i_{con1} , the numerator of the transfer function relating $i_{con1}(s)$ to $v_{dc1}(s)$ is:

$$s^2 + \left(\frac{R_L}{L_L} - \frac{P_{aco}}{C_{dc} v_{dco}^2} \right) s + \frac{1}{L_L C_{dc}} \left(1 - \frac{R_L P_{aco}}{v_{dco}^2} \right). \quad (10)$$

Sufficiently large values of inductance L_L and power operating point P_{aco} result in a pair of positive roots of , which are then reflected as a pair of right-half-plane (RHP) zeros in the plant $v_{dc1}(s)/i_{con1}(s)$. RHP zeros pose several fundamental limitations including high-gain instability, bandwidth limitation and inverse response [21]. Increasing the DC inductance or the inverting power of the power sink increases the possibilities of RHP zeros and degrades the controllability of the DC link. The effect of DC inductors on MTDC stability is highly dependent on the DC power flow, particularly the VSCs in constant power control mode.

With the DC inductor size varying from 0 to 150 mH, trajectories of selected closed-loop eigenvalues of the four-terminal model under two power flow conditions are shown in Fig. 12. The increase of L_{CB} reduces the oscillating frequencies and damping of the poles associated with the DC network. Using a larger L_{CB} has a more significant destabilizing impact on the PF2 scenario than the PF1 scenario. A low-frequency dominant mode migrates into the RHP and renders the closed-loop system unstable for the PF2 case, where both converters operate as inverters in constant power control mode and impose virtual negative admittances.

Under scenarios PF1 and PF2, frequency responses of the open-loop plant model with respect to VSC4 operating in droop control are presented in Fig. 13, for the four-terminal models with and without DC breaking inductors of 100 mH [25]. The scenario PF2 always has a larger phase lag than PF1 above 4 Hz due to the RHP zeros caused by the power flow direction. This implies that, with identical control settings, the system with fewer inverters in constant AP control mode is likely to have better stability margins especially phase margins, and be more robust to unmodeled high-frequency dynamics.

The introduction of the 100 mH inductor into the system significantly amplifies the frequency-domain peaks. The loop transfer function $L(s)$ in this case is therefore more likely to cross 0 dB at these frequency peaks and this could severely degrade the phase margin and may cause instability, especially when relatively high-gain controllers are employed. The DV controller gain should be sufficiently low around these resonant frequencies to allow acceptable stability margins.

B. DC Cable Modeling

The impact of DC cable modeling on MTDC stability has been neglected in a majority of previous literature. The eigenvalues of the MPIC-based and the CPIC-based test system models are shown in Fig. 14. The high-frequency DC network modes resulting from the CPIC-based model are located quite close to the imaginary axis, whereas the DC system modes of the MPIC-based model have much better damping. The dominant poles in Fig. 14 show that, with identical controllers, the closed-loop model based on the CPIC model may have much poorer stability than the MPIC based model. The CPIC-based model also exhibits more and sharper high-frequency resonant peaks, which could cause high cross-over frequencies and negative phase margins. With respect to VSC3 using the Type 3 droop control, the frequency responses of the MPIC-based and CPIC-based plant models are compared in Fig. 15. The frequency peak for the CPIC-based model around 30 Hz is much higher than the MPIC-based model and this is likely to result in a larger bandwidth and worse stability.

A more realistic MPIC model should therefore be considered since the CPIC model will exaggerate stability problems.

C. Short-Circuit Ratio

For a VSC system connected to a weak ac system, the PCC voltage could be sensitive to the active and reactive current variations of the converter system, and this leads to a more nonlinear relationship between the active power and d-axis current. Such nonlinearities can cause RHP zeros in the plant models of both the active power and DC voltage control for converters in rectifier operation [19]. The RHP zeros will locate closer to the origin for a system with a lower SCR and larger rectifying power. As the SCR of the droop-controlled VSCs of the test system varies from 5 to 1.7, the trajectories of the dominant closed-loop eigenvalues are shown in Fig. 16. The stability of the system using a Type 2 controller is not severely affected by the SCR variation. Conversely, the system based upon the Type 3 controller becomes unstable for $SCR < 1.9$ due to the poles being at 75 Hz. In this case, the RHP zeros caused by lower SCRs are more likely to be excited for a Type 3 droop due to the plant model having higher resonant gains than that for the Type 2 droop. This demonstrates a key advantage of the Type 2 control over Type 3 control in terms of robustness.

IV. DROOP CONTROLLER COMPARISONS

Most of the stability limitations addressed in Section III are generally applicable to all five types of DC voltage controls. The following comparative study investigates key stability features of the five droop implementations considered in this paper.

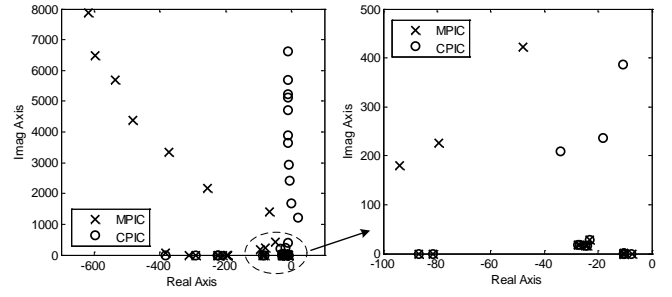


Fig. 14. Closed-loop eigenvalues of the four-terminals models based upon MPIC and CPIC models (PF1, Type 3 droop, $K_d=5\%$).

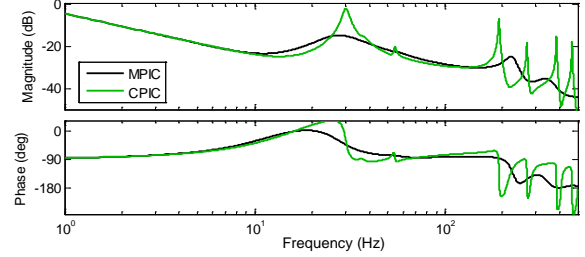


Fig. 15. Closed-loop eigenvalues of the four-terminals models based upon MPIC and CPIC models (PF1, Type 3 droop, $K_d=5\%$).

(a) System with $L_{CB}=0$ mH (b) System with $L_{CB}=100$ mH

Fig. 17. Frequency responses of the plant models $f_{vP4}(s)/i_{dA}^*(s)$, for Types 2 to 5 regarding droop control using VSC4, for systems with/without L_{CB} (PF2, $K_d=5\%$).

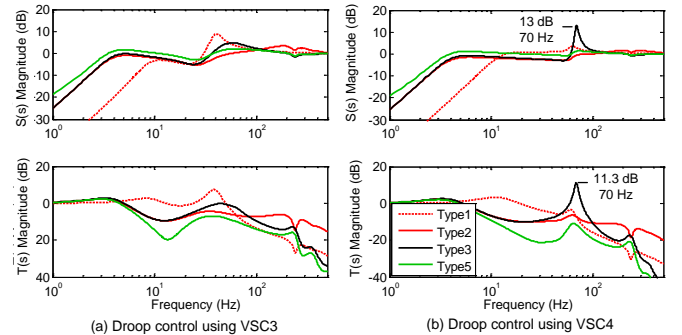


Fig. 18. Frequency responses of the SISO closed-loop $S(s)$ and $T(s)$ considering droop control using VSC3 and VSC4 respectively (PF2, $K_d=5\%$).

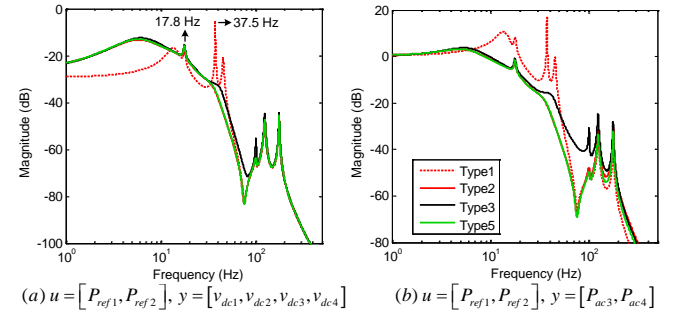


Fig. 19. Maximum singular value of the closed-loop disturbance models y/d with disturbances d and outputs y (PF2, $K_d=3.3\%$, $L_{CB}=100$ mH).

A. Selection of Output Signal

Control Types 2 to 4 have identical controller structure and are essentially differentiated by the selection of output signals, namely, ac power, DC power and DC current.

Frequency responses of the plant models for Types 2 to 5 are compared in Fig. 17, with respect to droop control implemented on VSC4. The differences of Type 3 V - P_{DC} droop

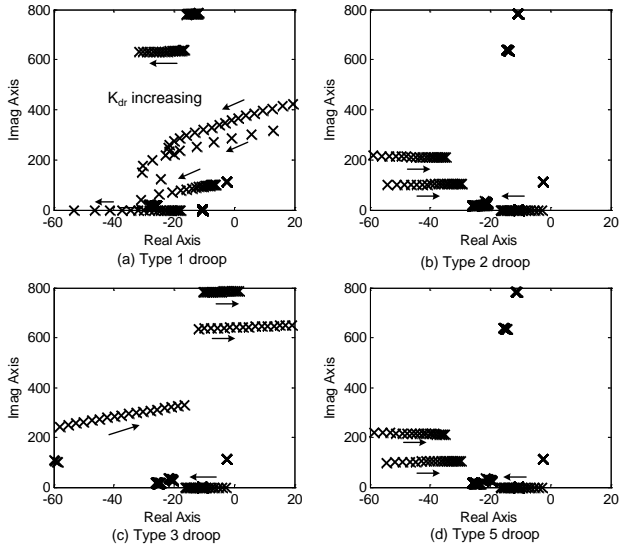


Fig. 20. Trajectories of closed-loop eigenvalues as K_{dr} varies from 1% to 20% (PF2, $L_{CB}=100$ mH).

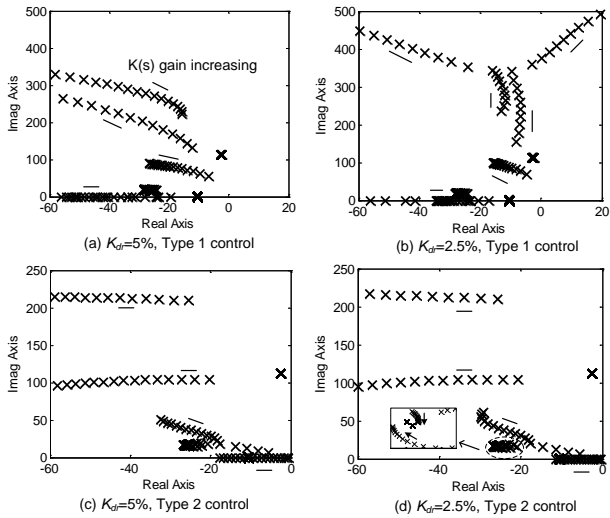


Fig. 21. Eigenvalue trajectories as the desired bandwidth varies from 4 Hz to 40 Hz for the design of AP or DV controller parameters (PF2, $L_{CB}=100$ mH).

and Type 4 $V-I_{DC}$ droop is negligible in the frequency domain, since the converter DC current and DC power contain almost identical dynamic information. Hence only Type 3 will be considered out of these two controller types for further study. Within low frequencies below 24 Hz, there is little difference between the plant models for Type 2 $V-P_{ac}$ droop and Type 3 $V-P_{DC}$ droop. However, the plant model for Type 3 tends to have a larger phase drop than the model for Type 2 as frequency increases. Consequently, with identical controller parameters, the closed-loop system for Type 3 will have a worse phase margin than Type 2, if the cross-over frequency is higher than 24 Hz. Moreover, the plant model for Type 3 also has a larger resonant peak at 53 Hz than that for Type 2. This together with the phase lag effect implies that $V-P_{DC}$ droop is likely to be more prone to high-gain instability than $V-P_{ac}$ droop.

Adding 100mH DC inductors does not impact the low-frequency response of the plant models for Type 2 and Type 3, as shown in Fig. 17(b). However, the plant model for Type 3 contains more and sharper resonant peaks above 100 Hz than

that for Type 2, since the signal P_{DC} is significantly affected by the overall DC network dynamics. Type 3 control is thus much more likely to be affected by modeling of the DC components such as DC cable and DC inductor.

DC voltage control using droop control can be decomposed into multiple SISO closed-loop systems. The SISO sensitivity and complementary sensitivity transfer functions $S(s)$ and $T(s)$ resulting from Types 1, 2, 3 and 5 are compared in Fig. 18(a) and (b), for droop control implemented on VSC3 and VSC4 respectively. The bandwidth of Type 1 control is much higher than the other droop types because the equivalent integral gain of Type 1 is much larger than the others, as the PI controller of Type 1 is identical to the AP controller. Therefore, Type 1 droop has better low-frequency disturbance rejection capability. However, it may be more vulnerable to RHP zeros and unmodeled dynamics due to its high bandwidth. The comparison between sensitivity peaks suggests that Types 2 and 5 tend to provide better stability than Types 1 and 3. Type 5 droop has slightly lower bandwidths than Types 2 and 3. However the complementary sensitivity $T(s)$ for Type 2 droop may not roll off sufficiently fast at high frequencies and may need additional low-pass filters to improve noise attenuation.

As shown in Fig. 18(b) when considering droop control implemented on VSC4, frequency-domain peaks of $S(s)$ and $T(s)$ at 70 Hz for Type 3 control are significantly higher than the others. This indicates that a closed-loop system utilizing the Type 3 control structure gives a much poorer stability and robustness under this condition. The large gain of the plant $L(s)$ at 55 Hz for Type 3 results in a high cross-over frequency which then seriously worsens the stability margins. This clearly shows a key weakness of using DC power rather than ac power as the feedback signal for droop control.

B. Droop Parameterization

This section is focused on analyzing the robustness of the candidate controllers with respect to droop parameterization.

The maximum singular value $\bar{\sigma}(G(j\omega))$, which represents the maximum gain of a multivariable system $G(j\omega)$ as a function of frequency, is a very effective frequency domain measure for MIMO performance and robustness [21].

In a MTDC system, the converters operating in AP control mode act as disturbances to the converters regulating DC voltage. The maximum singular value plots are shown in Fig. 19(a) and (b) respectively for the closed-loop model between the disturbances $[p_1^* p_2^*]$ and DC voltages, and the model between $[p_1^* p_2^*]$ and the powers of VSCs in droop control.

As shown in Fig. 19, the DC voltages are less perturbed by the disturbances at low frequencies for Type 1. However, this comes at a cost of more excessive usage of the active powers associated with VSC3 and VSC4. The Type 1 controller struggles to maintain system stability as the unacceptably high gain at 37.5 Hz implies very poor damping. Type 1 and Type 2 controls share identical output signals and are differentiated by the parameterization of $K(s)$, as the Type 1 control can be written in the form of Type 2 but with $K(s)=K^P(s)/K_{dr}$ instead of $K(s)=K^V(s)$. This implies that utilization of a relatively small droop K_{dr} will result in a high-bandwidth DV control loop if Type 1 is employed.

The singular value plots suggest that Types 2 and 5 have very similar frequency-domain characteristics. Slightly worse

disturbance rejection performance is provided by Type 3 in the frequency range of 35 to 100 Hz.

Fig. 20 shows the sensitivity of the closed-loop eigenvalues as the droop K_{dr} varies from 1% to 20%. As shown in Fig. 20(a) for Type 1 control, reducing the droop constant increases the DV control bandwidth and the overall system becomes more vulnerable to the constraints discussed in Section III. As shown in Fig. 20(c) for Type 3 control, the closed-loop system modes located above 35 Hz migrate towards the right-half s-plane as K_{dr} increases, since increasing of the weight of the DC power/current in $f_{v,p}$ creates larger resonant peaks in the plant. As shown in Fig. 20(b) and (d), the high-frequency modes for Types 2 and 5 are much more robust to droop variation than those for the other controllers, which is a clear advantage of using ac power or current for droop control.

When large droop constants K_{dr} are used, using DC power or current for droop control may result in high-frequency peaks in the plant and cause poor stability. For better stability, a low-pass filter (LPF) with an appropriately designed bandwidth is recommended to filter the measured DC power/current before feeding to Type 3 and 4 controllers.

The critically-damped dominant modes for Types 2, 3 and 5 migrate towards the origin as K_{dr} decreases. The application of very small droop constants can result in very slow modes and long settling time for Types 2, 3 and 5, as the interactions

between the integrators of droop controllers become stronger. Furthermore, the steady-state power sharing between droop-controlled terminals will be more dependent on DC system impedance for the use of a very small K_{dr} [12].

As the desired time constant τ_{des} that is used for AP or DV controller design varies from 40ms to 4ms, the eigenvalue trajectories of the systems employing Type 1 and Type 2 control are shown in Fig. 21. For the configuration of Type 1 droop with $K_{dr}=5\%$, increasing the gains of the AP controller $K^P(s)$ enhances both the damping and response speed of the system. Contrarily, as shown in Fig. 21(b) for the case with $K_{dr}=2.5\%$, increasing the gains of $K^P(s)$ could easily cause instability of the system. This effect implies that the controller parameters of Type 1 have to be retuned upon the variation of the droop constant. In contrast, for the Type 2 control, the eigenvalue trajectories for variations of tuning parameters of $K^V(s)$ are much less dependent on the selection of K_{dr} , as shown in Fig. 21(c) and (d). This shows another advantage of Type 2 over Type 1 that the parameterization of the main droop controller $K(s)$ is much more robust.

The key stability and robustness features of the five types of droop controller are summarized Table III.

TABLE III

COMPARISON OF THE KEY STABILITY FEATURES BETWEEN THE FIVE TYPES OF DROOP CONTROLLERS

Assessment Item	Type 1	Type 2	Type 3	Type 4	Type 5
Closed-loop bandwidth	High	Moderate	Moderate	Moderate	Moderate
Usage of converter power	High	Moderate	Moderate	Moderate	Moderate
Low-frequency disturbance rejection	Fast	Moderate	Moderate	Moderate	Moderate
Robustness to DC network resonances	Moderate/Poor	Moderate	Poor	Poor	Moderate
Robustness to droop gain variation	Poor	Good	Moderate/Poor	Moderate/Poor	Good
Robustness to DV PI gain variations	Poor	Good	Moderate	Moderate	Good

V. ACTIVE STABILIZING CONTROL

As the combined effect of DC power flow and DC impedance resonance could pose severe constraints on MTDC stability, there is a poorly damped mode at 17.8 Hz, as shown in Fig. 20 and Fig. 21, irrespective of the droop implementation. Such an oscillating mode is caused by the combined effect of constant power control and large DC inductors. An active stabilizing controller (ASC), which is a modified form of active damping control for inverter drive systems [26, 27], is proposed in this paper for MTDC systems to mitigate the negative admittance effect and inherently improve controllability and robustness of the DC voltage control. The key purpose of the ASC is to increase the dynamic damping by forming an additional feedback around the constant power control loop. According to Fig. 22, the active power reference P_{ac}^* is modified by the ASC as:

$$P^* = P_{ref} + K_a (v_{dc} - v_{dco}) \Rightarrow \Delta P^* = \Delta P_{ref} + K_a \Delta v_{dc} \quad (11)$$

where K_a is the stabilizing gain, v_{DC0} is the filtered DC voltage and P_{ref} is the steady-state power reference. By simplifying the closed-loop active power control to a first-order plant with a bandwidth of ω_p , the active power output of a converter in the ASC control mode can be represented as:

$$\Delta P = \frac{\omega_p}{s + \omega_p} \Delta P^* = \frac{\omega_p}{s + \omega_p} \Delta P_{ref} + K_a \frac{\omega_p}{s + \omega_p} \Delta v_{dc}. \quad (12)$$

Subsequently, the small-signal representation of the DC current source of the AVM can be linearized as:

$$\Delta i_{con} = \frac{\Delta P}{v_{dco}} - \frac{P_o}{v_{dco}^2} \Delta v_{dc} = \frac{\omega_p}{s + \omega_p} \cdot \frac{1}{v_{dco}} \cdot \Delta P_{ref} + \left(\frac{\omega_p}{s + \omega_p} \cdot \frac{K_a}{v_{dco}} - \frac{P_o}{v_{dco}^2} \right) \cdot \Delta v_{dc}. \quad (13)$$

As shown in Fig. 22, the stabilizing gain K_a is given as:

$$K_a = \frac{\alpha_p}{s + \alpha_p} P + K_s \approx P_o + K_s \quad (14)$$

where P_o is the converter power operating point, the filtering parameter α_p shall be sufficiently large, and K_s is named as

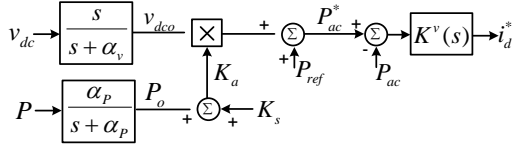
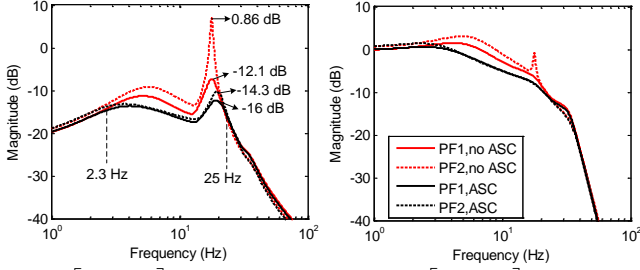
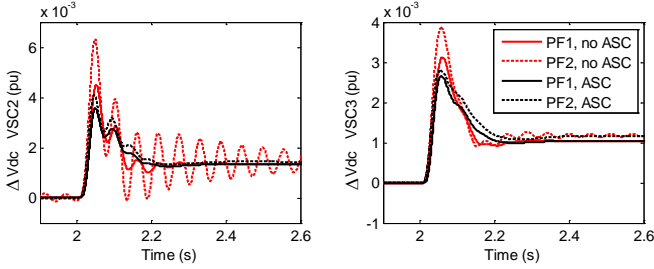


Fig. 22. Active stabilizing controller.

(a) $d = [P_{ref1}, P_{ref2}]$, $y = [v_{dc1}, v_{dc2}, v_{dc3}, v_{dc4}]$ (b) $d = [P_{ref1}, P_{ref2}]$, $y = [P_{ac3}, P_{ac4}]$ Fig. 23. Maximum singular value of the closed-loop disturbance models y/d with disturbances d and outputs y (PF2, $K_a=5\%$, $K_s=3$, Type 2, $L_{CB}=100\text{mH}$).Fig. 24. Responses of the dc voltage deviations of VSC2 and VSC3 to a 50 MW step decrease of P_{ref1} (PF2, $K_a=5\%$, $K_s=3$, Type 2, $L_{CB}=100\text{mH}$).

virtual admittance gain. The equivalent input admittance of the converter with ASC can then be derived as:

$$Y_{eq} = \frac{\omega_p}{s + \omega_p} \cdot \frac{K_a}{v_{dco}} \cdot \frac{P_o}{v_{dco}^2} = \frac{\omega_p}{s + \omega_p} \cdot \left(\frac{P_o + K_s}{v_{dco}} \right) - \frac{P_o}{v_{dco}^2}. \quad (15)$$

Natural admittance of 0 can be roughly achieved within the AP bandwidth by selecting $K_s=0$. However, K_s slightly larger than 0 is recommended since ω_p may not be sufficiently high to cover the resonant frequency of interest (i.e. 17.8 Hz in this case).

The impact of applying the ASC control instead of the constant power control to VSC1 and VSC2 is demonstrated in terms of closed-loop responses in Fig. 23, where the maximum singular values of the disturbance models of interest are shown. For the original system without the ASC, stability and disturbance rejection performance of the system for the PF2 scenario is significantly worse than that for the PF1 scenario. Replacing the typical AP control with the ASC enhances the stability of the system for the PF2 scenario, and significantly improves the robustness of the DC voltage control to power flow variations.

The four-terminal PF model is also built in PSCAD based on the AVM converter model and FD cable model to verify the analytical results using time-domain simulations. Responses of the deviations of v_{DC2} and v_{DC3} to a 0.05 pu step change of P_{ref1} are shown in Fig. 24, which agree very well with the frequency domain results shown in Fig. 23. The impact of ASC on the robustness improvement is evident, as the simulations for the two cases with ASC are both stable and well damped.

When large droop constants are used, utilizing DC power or current for droop control may result in high-frequency peaks in the plant and cause poor stability. For better stability, a low-pass filter (LPF) $H_f(s)$ with an appropriately designed bandwidth is recommended here for the power measurement of the Type 3 and 4 control, as shown in Fig. 25.

The impact of this additional LPF for Type 3 droop on the frequency responses of the closed-loop disturbance models is shown in Fig. 26. The corresponding eigenvalues of interest are shown in Table III. A second-order LPF with a bandwidth of 15 Hz is employed. Using the Type 3 droop with $K_{dr}=20\%$ causes a series of singular value peaks, which implies poor damping and instability at the associated resonant frequencies. The LPF used for DC power filtering is effective in terms of stabilizing the oscillatory modes at 52 Hz and 124 Hz. However the LPF is not able to improve the poorly damped low-frequency modes caused by the negative admittance effect. This issue is much more effectively dealt with by employing the ASC control for VSC1 and VSC2, as shown in Fig. 26.

With the system stabilized by the Type 3 controllers with LPF, responses of VSC1 and VSC3 to an ac fault at PCC2 are shown in Fig. 27, for three ASC control scenarios. The fault occurring at 2s caused 30% voltage sag at PCC2 and was cleared after 0.1s. A larger ASC is more effective in damping improvement but requires more usage of the converter power. DC voltages of the inverters in constant power control can be significantly more oscillatory than those converters in droop control, although this may not be a severe issue for systems without breaking inductors.

VI. CONCLUSION

In this paper, a general framework for the analysis of various droop control configurations employed for MTDC systems has been proposed. This framework is then used to compare leading droop configurations in terms of their impact on controllability, closed-loop stability, robustness and dynamic performance of the overall MTDC system.

The following stability limitations have been identified for the DC voltage control:

- 1) The negative admittance effect caused by inverters operating in constant power mode limits DC voltage control bandwidth and degrades both robustness and stability of the DC system.
- 2) The use of large DC inductors can severely deteriorate the controllability of the DC network and cause critical low-frequency resonances for any of the droop configurations.
- 3) Weak ac system connection can pose different bandwidth limitations on different types of droop controllers.

The analysis in this paper leads to the following design recommendations for DC voltage droop control:

- 1) All the five droop types can be applied with care. However, under severe plant constraints, Type 2 and Type 5 droop generally possess better stability and robustness than the others.
- 2) In comparison to the droop control based on ac power or ac current, the control based upon DC power or DC current has similar low-frequency dynamic characteristics. However, it is more vulnerable to high-frequency DC resonances, weak ac systems and large droop constants.
- 3) For Type 3 or Type 4 controls, to stabilize high-frequency oscillatory modes, the DC power or DC current is suggested to be appropriately filtered before it is fed to the droop controller.
- 4) The PI parameters of the droop controllers should be tuned based upon the DC voltage plant model rather than the active power plant model, to avoid aggressive dynamic response and improve the system robustness to droop gain variations.
- 5) Replacing active power control with the ASC control is very effective in mitigating the negative impedance effect and improving the robust stability with respect to power flow variations.

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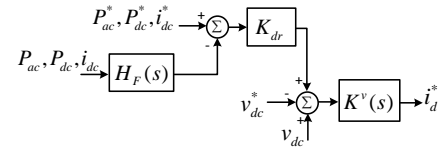
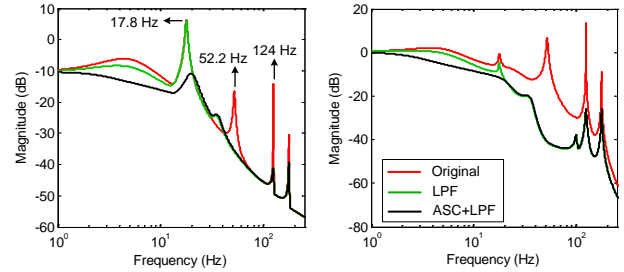


Fig. 25. Modified droop controller with additional filtering function.



(a) $d = [P_{ref1}, P_{ref2}]$, $y = [v_{dc1}, v_{dc2}, v_{dc3}, v_{dc4}]$ (b) $d = [P_{ref1}, P_{ref2}]$, $y = [P_{ac3}, P_{ac4}]$

Fig. 26. Maximum singular value of the closed-loop disturbance models y/d with disturbances d and outputs y (PF2, $K_{dr}=20\%$, $K_i=4$, Type 3, $L_{CB}=100$ mH).

TABLE IV

SELECTED EIGENVALUES CORRESPONDING TO THE CASE SHOWN IN FIG. 26

Mode	Original	LPF	ASC+LPF
1	$0.252 \pm j781$	$-11.1 \pm j782$	$-11.1 \pm j782$
2	$28.3 \pm j643$	$-13.1 \pm j630$	$-13.1 \pm j630$
3	$-5.43 \pm j327$	$-23.4 \pm j222$	$-23.6 \pm j224$
4	$-2.55 \pm j112$	$-2.55 \pm j112$	$-18.4 \pm j126$

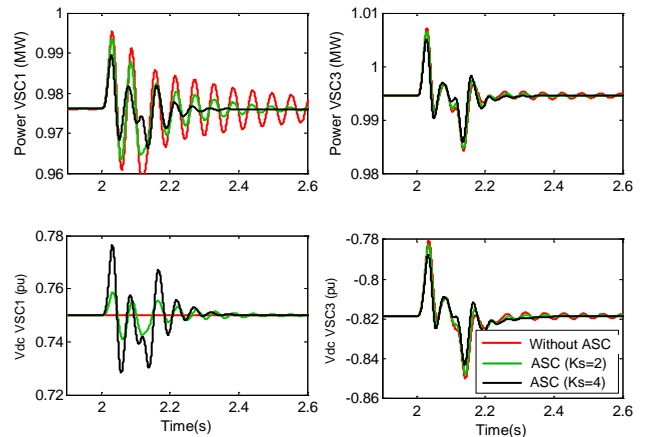


Fig. 27. Responses of VSC1 and VSC3 to an ac fault occurring at PCC2 (PF2, $K_{dr}=20\%$, Type 3, $L_{CB}=100$ mH).

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